Advances in 3D CMOS Sequential Integration

P. Batude, M. Vinet, A. Pouydebasque, C. Le Royer, B. Previtali, C. Tabone, J.-M. Hartmann, L. Sanchez, L. Baud, V. Carron, A. Toffoli, F. Allain, V. Mazzocchi, D. Lafond, O. Thomas, O. Cueto, N. Bouzaida, D.Fleury[2], A. Amara[1], S. Deleonibus and O. Faynot.

CEA, LETI, MINATEC, 17 rue des Martyrs F38054 Grenoble, France
[1]ISEP, 21 rue d'Assas, 75270 Paris cedex 06 France
[2] STMicroelectronics, 850 rue Jean Monnet F38926 Crolles, France
Tel: 33 438782329, Fax: 33 438783034, e-mail: perrine.batude@cea.fr

Abstract

For the first time 3D sequential CMOS integration turns up to be an actual competitor for sub 22nm technology nodes. Thanks to the original use of molecular bonding, high quality top Si active layers are obtained. Thermally robust bottom salicide goes through the whole top FET processing without any significant sheet resistance degradation. The low temperature integration of raised source and drain for top layers is demonstrated. A decrease by 4Å of the Equivalent Oxide Thickness is measured when a low thermal budget process is implemented. The electrostatic coupling between stacked FETs is demonstrated thanks to an ultra thin inter layer dielectric thickness of 60nm. It leads to a threshold voltage dynamic shift of 130mV enabling SRAM stabilization.

Introduction

3D integration generates great interest to solve the fundamental limits of scaling *e.g.* increasing delay in interconnections [1], development costs and variability [2]. 3D sequential integration, by opposition to parallel (or back-end or TSV 3D integration) is the only technological option enabling to fully benefit from the third dimension potential at the transistor scale thanks to its high alignment precision (σ_{SEQ} ~10nm[3] compared to σ_{TSV} ~0.5µm [4]). The sequential processing of bottom and top FET is however challenging because of the potential detrimental impact on bottom FET of the top FET processing. In this paper, we demonstrate the possibility of obtaining regular 2D performances within a 3D sequential integration scheme. We further investigate the unique features of low temperature process. Finally, we quantify for the first time, the electrostatic coupling between the layers.

Device fabrication

P and N FDSOI transistors with 5mn HfO_2 and TiN/Poly-Si N^+doped gate stack were fabricated on the bottom layer (fig.1). Thin Inter Layer Dielectric (ILD) was deposited and planarized on top of these transistors. A low temperature (200°C) molecular bonding of SOI substrates was used to obtain perfect quality top active layers. Depending on pre-bonding planarization, thin Inter-Layer Dielectric (ILD) of 110 nm (fig.2) and ultra Thin ILD (UTILD) of 60nm have been obtained. Top MOSFETs have been then processed with an overall thermal budget limited to 600°C. Solid Phase Epitaxy (SPE) at 600°C has been used for dopant activation.

Results and discussion

Reaching individual 2D transistor performances

To be a serious alternative to regular 2D transistors, 3D sequential integration has to demonstrate its ability to integrate the same performance boosters. Use of low temperature molecular bonding to realize top active layers is a remarkable way to fit with this requirement. It indeed allows classical bottom layer salicidation which has not yet been achieved with recristallization or growth techniques due to intrinsic technological challenges [5-7].

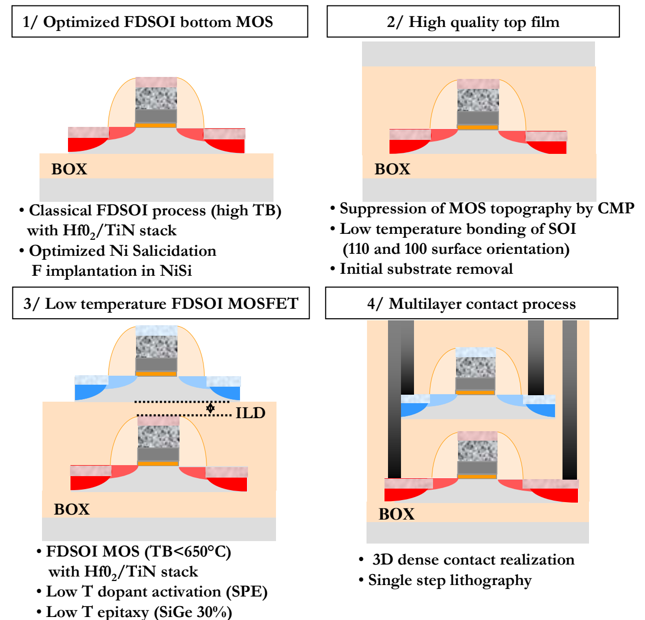


Fig.1: Description of the process flow

Thanks to Fluorine implantation into NiSi, we manage to design a morphologically robust salicide (fig.3-a). Fig.4 shows the beneficial impact of F on the sheet resistance of blanket wafers as a function of annealing time @ 600°C. After a complete top integration (thermal budget is summarized fig.3-b) R_{sheet} of NiSi(F) is still around its original value (12 to 14Ω/sq) which is just above the standard NiSi R_{sheet} used for the top FET, fig.5. A second unique advantage of bonding is that it allows independent optimization of the stacked layers: channel material [7, 8] and/or crystalline orientation of top and bottom FETs. For the first time we were able to process independently (110) PFETs on top of (100) NFETs. Fig.6 shows the measured mobility of (110) PFETs in the <100> direction. Best mobility values are

expected in the <110> direction [9] and can be reached thanks to a 90° rotation of the top wafer during bonding. Finally, in order to compete for the 22nm node, the integration of raised source and drain (RSD) is mandatory for top and bottom layers in sequential 3D. For this purpose a specific low temperature epitaxial growth was developed, fig.7. Pure Si was replaced by SiGe to increase growth rate for T<650°C. It allows reaching $4nm.min^{-1}$ for 30% of Ge and can be further increased with higher Ge contents. To tackle independent optimization of N and PFET on separated layers, in situ B doped SiGe RSD were also demonstrated, fig.8 and have recently proved their efficiency for 22nm PFETS [10]. Solid Phase Epitaxy was also investigated for CMOS integration purpose in the top layer. In that case, extraction of access resistance thanks to the Y-function method leads to a global access resistance around 400 Ω.µm, *i.e.* $R_{source} \approx R_{drain} \approx 200\Omega.\mu m$, fig.9. These values are confirmed using the Rtot (1/β) method proposed in [11] and are in line with state-of-the-art technologies [12]. It proves that SPE is still efficient for thin films and leads to high dopant activation levels.

Unique low temperature features

We have already shown that the reduced thermal budget (overall temperature kept below 600°C) used for the top layer leads to highly controlled short channel effects [8]. It also yields thinner EOT than its Rapid Thermal Annealing counterpart. Capacitance measurements were performed on N and PFETs of top and bottom layers, fig.10. With a 5nm HfO_2 gate dielectric for both types of devices we observed a 4Å EOT reduction: 1.5nm (resp. 1.6nm) for top NFET (resp. PFET) compared to 1.9nm (resp. 2nm) for bottom NFET (resp. PFET). The EOT decrease is due to the reduction of interfacial oxide growth as shown on the cross sectional TEM images of the two gate stacks (fig.11). Gate current was plotted as a function of EOT (fig.12). This figure of merit clearly underlines the advantage of low thermal process: J_G is around 5 decades lower than the SiO_2 reference curve.

3D specificities

We performed a complete optimized 3D integration ((110) was used for top PFETs). $I_D(V_G)$ are shown on fig.13. They exhibit no degradation of bottom characteristics due to top integration process. The observed shift of the threshold voltage between top and bottom layers is attributed to the PVD TiN work function increase with final annealing temperature. $I_D(V_D)$ output characteristics show well behaved devices for top and bottom layers (fig.14 and 15). A functional equilibrated inverter was demonstrated with (110) PFET on top of (100) NFET, fig.16. We also have fabricated 3D SRAM with (100) NFET stacked on (100) PFET as described in fig.17. The functionality of the SRAM is tested using the cycle of polarization described in fig.18. The measurement displayed in fig. 19, evidence that the cell can be written, and maintain the information in read and retention regime. The cell shows a symmetrical behavior either a '0' or a '1' is memorized.

The unique 3D electrostatic coupling between layers was quantified: depending on the targeted ILD the top transistors can be considered either as FDSOI with thick BOX (thin ILD, fig 2 and 17) or as Double Gate like devices (ultra thin ILD, fig 18 and 19). In that case a 130mV v_{TH} shift is observed when the top NFET lies above a bottom transistor as compared to the isolated case (Φ_m of the bottom gate is the one of N+ doped polysilicon *i.e.* 5.1eV). It demonstrates that the threshold voltage of top FETs can be dynamically tuned by biasing the bottom FET. This characteristic presents strong interest for the stabilization of SRAM cells [13, 14].

Conclusion

In this 3D sequential integration, we demonstrate our ability to integrate salicided access in the bottom layer. (110) PFETs are processed on (100) NFETs and low temperature RSD are developed for the top layers. In addition, the use of low thermal budget process leads to a reduced interfacial oxide layer together with very low gate current. For the first time the electrostatic coupling between the layers is demonstrated as a function of ILD thickness (an up to 130mV V_T shift was observed).

Acknowledgments

This work was partly supported by the French National Research Agency (ANR) through Carnot funding and by the ST-IBM-LETI Alliance program.

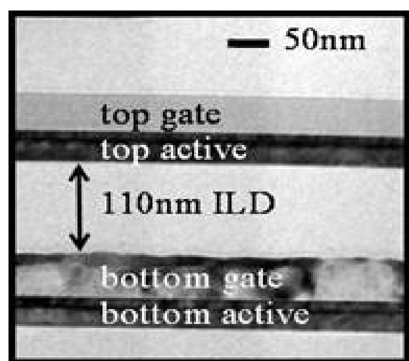
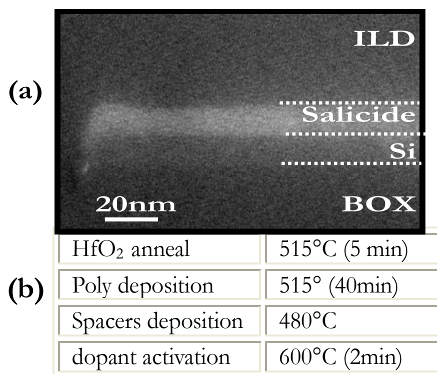


Fig. 2: TEM cross section of two stacked transistors featuring a 110nm thick ILD. Top and bottom active thickness are around 30nm.



HfO_2 anneal	515°C (5 min)
Poly deposition	515° (40min)
Spacers deposition	480°C
dopant activation	600°C (2min)

Fig.3: a - SEM cross-section of bottom FET source after top FET process without any dewetting evidenced. b- Summary of the thermal budget seen by the bottom FETs.

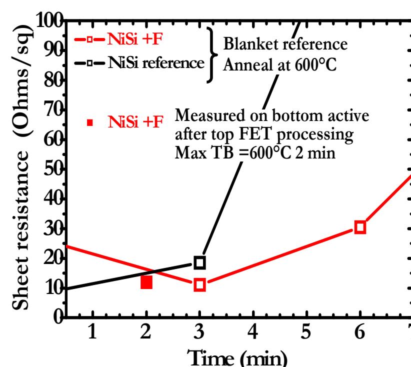


Fig. 4: Influence of F implantation in NiSi in term of electrical stabilization when submitted to 600°C anneal (blanket wafers) and comparison with measured results on bottom FET active (VanderPaw structures) after top FET processing.

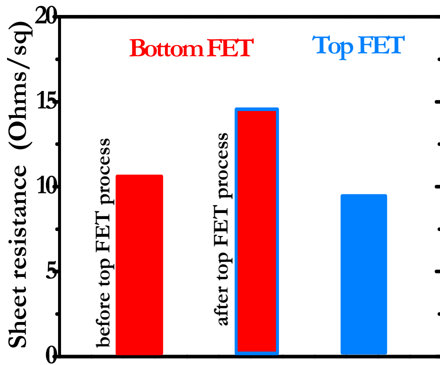


Fig. 5: Sheet resistance measurements of bottom salicide (before and after top FET processing) and of top salicide.

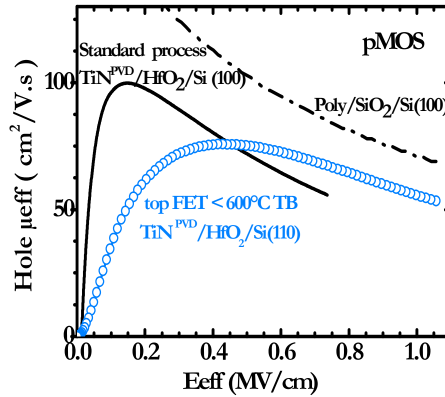


Fig.6: Hole effective mobility extraction by split CV for top PFET processed on (110) orientation.

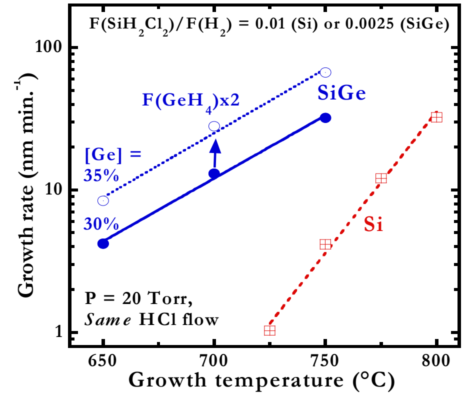


Fig.7: Epitaxial growth rate vs temperature. Replacing Si by SiGe enable to achieve reasonable growth rates at 650°C.

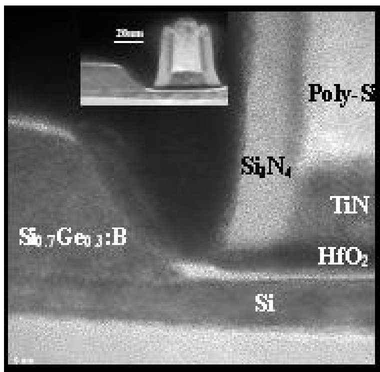


Fig.8: TEM cross-section of FET with 650°C SiGe raised sources and drains.

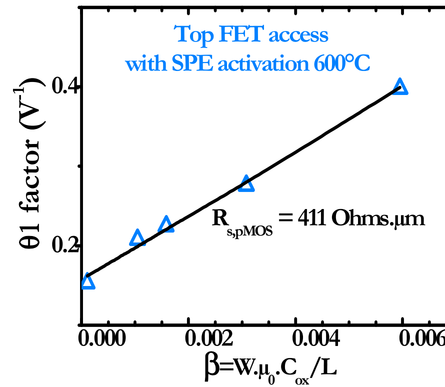


Fig.9: Access resistance extraction using Y- function method on top FET (SPE at 600°C).

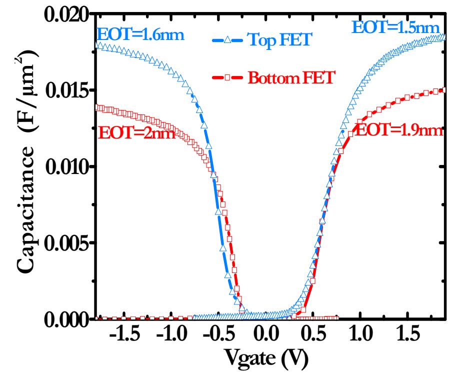


Fig.10: C(V) characteristics of bottom and top FETs. 4Å EOT reduction is observed with low TB

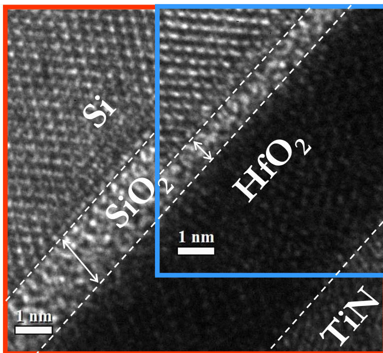


Fig.11: TEM cross-section of top and bottom oxides showing reduction of interfacial oxide growth.

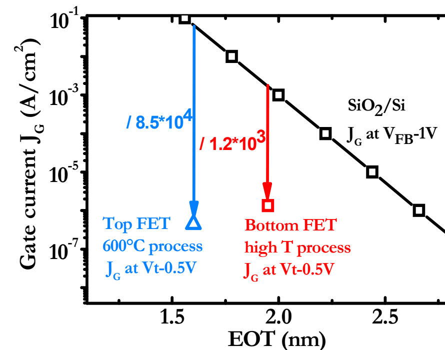


Fig.12: Figure of merit of top and bottom oxides underlining the interest of low T process.

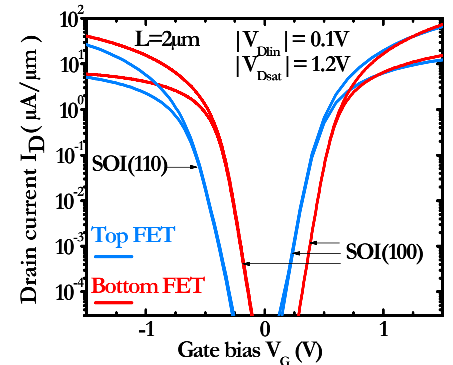


Fig.13: I_D-V_G characteristics of bottom and top FETs.

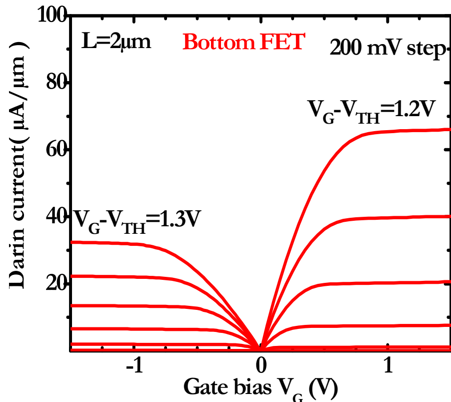


Fig.14: I_D-V_D characteristics of bottom FET

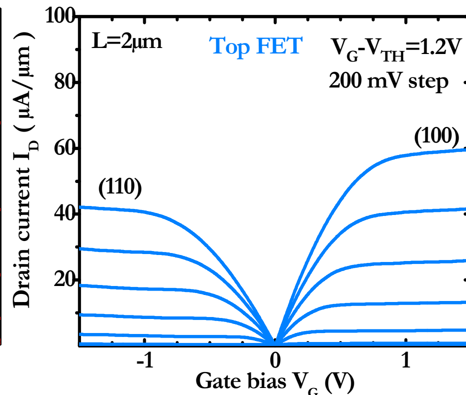


Fig.15: I_D-V_D characteristics of top FET

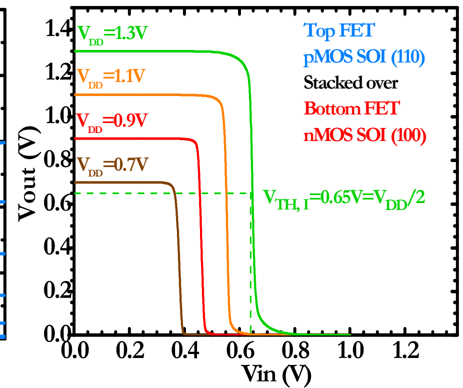


Fig.16:Transfer Voltage characteristic of an inverter: top SOI (110) pFET and bottom SOI (100) nFET

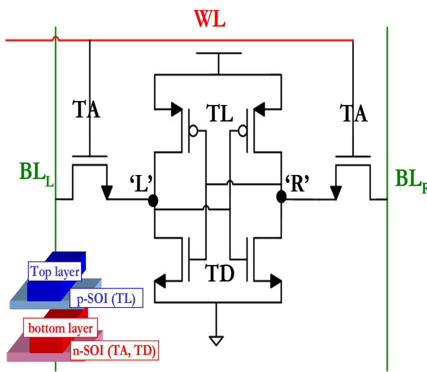


Fig.17: Description of the 6T SRAM cell demonstrated. pMOS load FETs are stacked over nMOS drive and access FETs

	Regime	WL	BL_L	BL_R
1	Writing 'L'='0'	V_{DD}	V_{DD}	0
2	Retention	0	V_{DD}	V_{DD}
3	Reading	V_{DD}	V_{DD}	V_{DD}
4	Writing 'R'='0'	V_{DD}	0	V_{DD}
5	Retention	0	V_{DD}	V_{DD}
6	Reading	V_{DD}	V_{DD}	V_{DD}

Fig.18: Description of polarization of the BLs and WlLwhen testing the functionality of the SRAM in reading, retention and writing regimes.

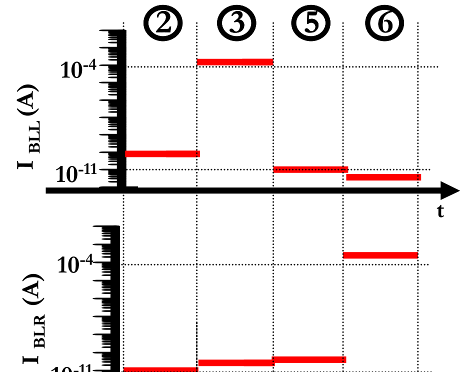


Fig.19: BLs current measurement of the 3D SRAM cell fabricated, in the different regimes described in fig.18.

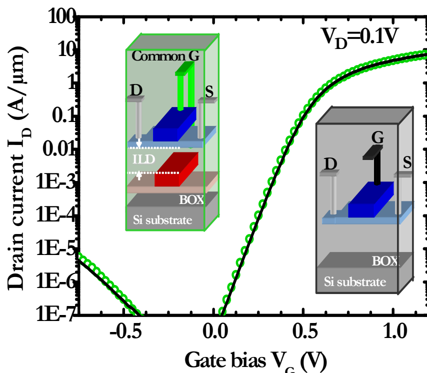


Fig.20:I_D-V_G characteristics of top transistors with T_{ILD}=110nm. No modification is observed when the configuration of the top FET changes (above bottom FET or not)

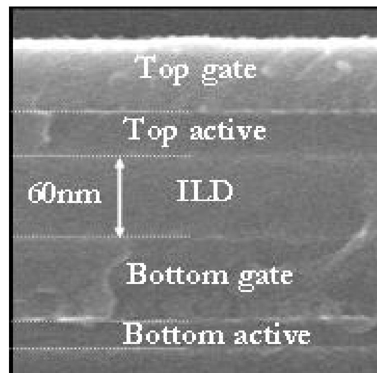


Fig.21: SEM cross section of an 3D stack with Ultra Thin ILD (UTILD)

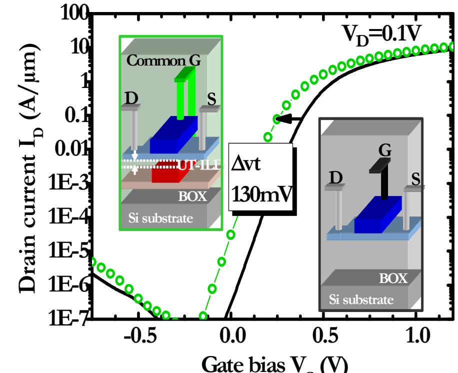


Fig.22:I_D-V_G characteristics of top transistors with T_{ILD}=60nm. Ultra thin ILD allow to modify the top FET threshold voltage

References

[1] K. Banerjee et al, *IEEE 01*, vol.89 p.602, [2] S-M. Jung et al, *VLSI 05*, pp220, [3] P. Batude, *ECS 08*, VO 16 pp4,[4] A-W. Topol et al, *IEDM 05*, p.352, [5] Y-H. Son et al, *VLSI 07*, pp80, [6] S-M. Jung et al, *VLSI 07*, pp82, [7] J. Feng et al, *EDL 08*, Vol.27 NO11 pp911, [8] P.Batude *et al.*, p.166, VLSI 09, [9] Packan *et al.*, p1 ,IEDM08 ,[10] K. Cheng *et al.*, p.212, VLSI09, [11] D. Fleury et al., EDL, V30, No9, 2009 [12] K. Yako *et al.,* IEDM, p. 909, 2008, [13] P.Batude *et al.,* ICICDT, p. 281 2008, [14] O.Thomas *et al.,*ICICDT, 2009