AMS Design Flow Highlights for FD-SOI

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Outline

- Introduction
- AMS Is The Differentiator - regardless of FDSOI or FinFET
- Circuit Verification Challenges & Solutions
- AMS Verification: Electrical, Functional, and Physical
- Summary
Today, Platforms Define The Winners
Platforms Are Rapidly Going Into Deep Nanometer
## IC Market Segment Summary

<table>
<thead>
<tr>
<th>Terminology</th>
<th>AMS IC</th>
<th>nm AMS IC</th>
<th>SoC</th>
<th>Memory IC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Analog-Rich</td>
<td>Analog Mixed-Signal ICs</td>
<td>Digital Mixed-Signal ICs</td>
<td>Standalone Memory ICs</td>
<td></td>
</tr>
<tr>
<td>Analog-dominated ICs ASSPs and Catalog ICs</td>
<td>Analog-dominated mixed-signal ICs, ASSPs</td>
<td>Digital-dominated mixed-signal SoCs, CPUs, Aps</td>
<td>Non-volatile Memory (FLASH) and DRAM</td>
<td></td>
</tr>
<tr>
<td>0.5u – 130nm</td>
<td>130nm – 28nm</td>
<td>90nm – 10nm</td>
<td>Dedicated Nanometer</td>
<td></td>
</tr>
<tr>
<td>Automotive Consumer Industrial Power ICs Sensors Clocking ICs LED Lighting Optical ICs Standard analog</td>
<td>Wireless Transceivers GBE Transceivers CMOS image sensors Multimedia ICs MCU-based ICs Market-specific ASSPs (auto, industrial, medical, etc)</td>
<td>CPUs SoCs Application Processors Baseband Processors GPUs Network Processors Security Processors (included embedded SRAM)</td>
<td>Non-volatile Memory DRAM ...</td>
<td></td>
</tr>
<tr>
<td>TI, STMicro, Analog Devices, Maxim, Infineon, ON Semi, Skyworks</td>
<td>QCOM, MTK, BRCM, Marvell, Mstar, IDT, Inphi, Motorola, Spreadtrum, NXP, ST SiLabs, Sony</td>
<td>Apple, Samsung, QCOM, Intel, AMD, Oracle, Fujitsu, MTK, NVIDIA, BRCM, Spreadtrum, Cavium, Altera, Xilinx</td>
<td>Samsung, Micron, SKHynix, Toshiba, Intel</td>
<td></td>
</tr>
<tr>
<td>Highly Fragmented ICs</td>
<td>Analog dominates flow</td>
<td>Digital dominates flow</td>
<td>Yield dominates flow</td>
<td></td>
</tr>
</tbody>
</table>
Using Moore vs More than Moore for Platform Control

Source: GloFo
What About Mixed-Signal Integration?

Mixed-signal integration is simply the next step in integration
— Moore or “More than Moore”

Motivation Is Cost (really?)
— Establish differentiation via performance, power, cost, features
— Establish differentiation via specific or uniquely integrated features

Motivation Is Platform Control
— Control integration of key functions in a platform
— Control of silicon bill of materials (BOM)
— Control evolution of features on the platform
— Software lock-in!
FD-SOI vs. FinFET - Cost vs. Performance Comparison

20nm Die Costs at 100mm² and 200mm²

Bulk FD SOI projected to have lower unit cost than FinFET due to higher FinFET process complexity and expected lower die yield

April 30, 2014
28nm FD-SOI High-Performance ADCs: 56 GS/sec 6-bit Charge-Mode Interleaved SAR ADC

- The MOORE Path
- Ultra-fast CMOS ADC: the enabling technology for 100Gbps Ethernet and OTU-4 transport systems using coherent receivers.
- Coherent receiver needs four 56GSa/s ADCs and a Tera-OPS DSP that dissipates only tens of watts.
- Ultra-low power and cost drive an integrated single-chip solution in 28nm FD-SOI integrating an ultra-fast CMOS ADC with ultra-high-performance DSP
- Circuit Simulation: transient, transient noise, and extracted sims with S-params
- Higher-speed short-haul links coming – requires driving down power and cost even lower
28nm FDSOI CIS Mixed-Signal Engine: Top-of-the-line Pixel Array with High Performance ISPProcessor

- The “MORE THAN MOORE” Path
- Stacked Back-Illuminated CMOS Image Sensor: the enabling technology for next generation CIS systems
- Increasing demand for pixel-customization for new advanced features (global shuttering, etc)
- Increasing demand for advanced digital signal processing for new features (recognition, depth sensing)
- Ultra-low power and cost drive a More-than-Moore approach with SIP solution in 28nm FD-SOI for logic
- Circuit Simulation:
  - Transient, device noise, multi-cycle-operation, and extracted sims
  - Multi-technology simulation required for die-to-die

Source: ISSCC 2014
AMS: Expected Redesign Effort Put Significant Pressure on Circuit Design and Verification Tools

**IP Porting Efforts:**

<table>
<thead>
<tr>
<th>Type of Foundation IP</th>
<th>Expected Redesign Effort</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standard Cell Libraries</td>
<td>Very Limited (*)</td>
</tr>
<tr>
<td>Memory Compilers</td>
<td>Very Limited (<strong>,</strong><em>,</em>)</td>
</tr>
<tr>
<td>I/Os</td>
<td>Limited (*)</td>
</tr>
<tr>
<td>Analog and Mixed Signal</td>
<td>Limited to More Significant</td>
</tr>
</tbody>
</table>

(*) : Assuming the “worthwhile benefits at fastest time-to-market” approach is favored
(**) : Assuming availability of suitable ‘native VT’ – see 4.2

Source: SOI Consortium, “Considerations for Bulk CMOS to FDSOI Porting,” 2011
Investing In AMS…and Across Verification: Functional, Electrical, and Physical for FDSOI

- **Functional verification**
  - Questa
- **AMS Verification**
  - Electrical Verification
- **Physical verification**
  - Calibre

**Leverage**
- Full language support
- Full feature support
- Advanced debug
- Powerful tie to reqt. tools

**Leverage**
- Faster and higher capacity
- Device noise analysis
- Multi-technology sim
- Variability analysis

**Leverage**
- PERC
- xACT, mPower, RealTime
- Foundry position
- Large installed base
FDSOI & Circuit Simulation

- Requires a conventional flow
- Based on a support of a proven compact model UTSOI, developed by CEA/LETI & ST:
  - To integrate in circuit simulators
  - To qualify with circuit simulators and DK releases
  - To deploy for a large set of use cases (Cell Characterization, Design & Verification of AMS IPs and SoC)
- UTSOI models and Circuit Simulation:
  - PSP based model
  - Four terminal transistor model
  - Models equations modified to account for FDSOI technology

UTSOI is used to describe 28FDSOI MOSFETs
  - ST – LETI Co-development

Excerpt from: 28 & 20nm FDSOI Technology Platforms
Giorgio Cesana  ST Microelectronics Technology R&D

Ref.: « UTSOI model: a physical and Si calibrated model; O. Rozeau, O. Faynot (CEA/LETI), Hsinchu FDSOI Workshop, 2011 » and numerous publications from LETI
FDSOI & Mentor AMS Verification

- Speed was the challenge, and both Eldo and AFS deliver high-performance:
  - First UTSOI model version v1.1 (Verilog-A) available for circuit simulators in May 2011
  - First production release within Mentor Graphics AMS tools in October 2011
  - First large scale characterization campaign started in March 2012 at large FD-SOI partner, following the qualification of the characterization flow
  - Model « maturation » much faster than regular CMC compact models:
    - Industrial drive from ST
    - Strong research capabilities at CEA/LETI
    - Close collaboration of Grenoble ecosystem
  - AFS Platform from BDA supported FDSOI following customer requests from Asia and North America
  - Following acquisition of BDA, integrated support for FDSOI across all simulation platforms in Mentor Graphics
Eldo – Comprehensive Solution for Analog IC

- Reliability
  - NBTI
  - HCI, TDDB
- Thermal Analysis
- Transient Noise
- Process Variation
- Leakage Current

Quality

Yield
**Eldo → Targeted Segment & Applications**

- **AMS IC and nm AMS IC Segment Targeted**
  - Analyses-rich analog simulator
  - Diagnostic simulations
  - SPICE Formats
    - Eldo netlists/models
    - HSPICE & Spectre compatibility for netlists/models
  - Processes
    - CMOS 0.5μ to 28nm (Bulk, SOI)
    - Bipolar, BiCMOS, DMOS, SiGe, GaAs, etc.
    - Foundry certified (HSPICE & Spectre models)
  - Target Applications → Automotive IC
    - Power Discrete & Modules
    - Sensors & Actuators
    - Motor Drivers
    - PMICs & Switchers
    - Network Transceivers

- **Applications**
  - Capacity: Up to 1M elements analog
  - Performance: 2-5x traditional SPICE
  - Accuracy: Foundry certified (golden SPICE)
  - Advanced Analog-Centric Circuit Verification
  - Mixed-Signal: Comprehensive, accurate AMS
Accelerated SPICE-Accurate Simulations

- Eldo Premier – dramatically accelerates transistor-level SPICE-accurate simulation of large circuits
  - SPEED: >3x on average, up to 20x
  - ACCURACY: Within user-defined tolerance
  - CAPACITY: ~1M devices, i.e. ~10x Eldo Classic

- Brand new matrix solver and algebra, hierarchical with smart parasitic reduction
- Classic/Premier engine auto-select
- Selectable accuracy vs. performance global/local tuning
- Available with Questa ADMS Premier
- Development focus on performance improvement for SOI and BCD processes
What’s New in Performance

- Eldo Premier Transient Noise Performance Improvement
  - Eldo Premier NOISETRAN analysis has been optimized to provide faster simulation run time (compared to previous versions) without any compromise on result accuracy
  - Target circuits: PLLs

- Local Sub-circuit Tolerance in Eldo Premier
  - .LOCALTOL allows Eldo Classic & Premier to improve performance on some blocks and tighten accuracy on others

- Aging Simulations Performance Improvement
  - New optimized aging scheme for Eldo Classic and Premier
  - 2.5X faster on average (15.1 vs. 14.1) without any accuracy loss
Advanced Circuit Analysis Supporting FDSOI

- Eldo Shows You Where and Why
  - Hierarchical power analysis
  - Transient sensitivity and noise
  - Hi-Z nodes detection
  - Built-in optimizer
  - Circuit profiling
  - Advanced post-processing
  - Advanced safe operating analysis
  - DSPF & SPEF parasitic back-annotation
What’s New in Statistical Simulations

- Monte Carlo Acceleration for Rare Events

```
.MC SAMPLING=RND | LHS | QMC | SSD | ISMC
+ [IS_MAXITER=MAX_ITER] [IS_RTOL=RVALUE]
```

- Default pseudo-random MC cannot be used for small probabilities (e.g. \(1e^{-4} < P_{\text{fail}} < 1e^{-10}\)) as sample size would be too large

- Purpose is to estimate accurately and efficiently:
  - Very low failure probabilities (\(P_{\text{fail}}\))
  - and/or associated quantiles (\(Q_{\text{fail}}\))

- Applications in FDSOI
  - SRAM
  - Standard Cells
  - (Analog IPs)

<table>
<thead>
<tr>
<th>Circuit</th>
<th>Variables</th>
<th>Runs</th>
<th>Proba/Quantile</th>
<th>Estimation</th>
<th>Accuracy @95%</th>
<th>Speedup</th>
</tr>
</thead>
<tbody>
<tr>
<td>SRAM bit-cell</td>
<td>12</td>
<td>9040</td>
<td>Proba</td>
<td>3.7e-11</td>
<td>9%</td>
<td>1.4e9</td>
</tr>
<tr>
<td>SRAM bit-cell</td>
<td>12</td>
<td>7020</td>
<td>Quantile</td>
<td>178.7</td>
<td>0.3%</td>
<td>100e6</td>
</tr>
<tr>
<td>SRAM cell</td>
<td>23</td>
<td>10060</td>
<td>Proba</td>
<td>1.7e-9</td>
<td>9.9%</td>
<td>22e6</td>
</tr>
<tr>
<td>VCO</td>
<td>1500</td>
<td>40080</td>
<td>Proba</td>
<td>1.4e-4</td>
<td>9.3%</td>
<td>70X</td>
</tr>
<tr>
<td>Memory</td>
<td>2096</td>
<td>115340</td>
<td>Proba</td>
<td>5.2e-6</td>
<td>10.4%</td>
<td>59e3</td>
</tr>
<tr>
<td>Standard Cell</td>
<td>98</td>
<td>7060</td>
<td>Proba</td>
<td>5.7e-5</td>
<td>9.9%</td>
<td>950X</td>
</tr>
</tbody>
</table>
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Antenna Protection Cells (DRC)

- In bulk CMOS technology, protection against “antenna-effects” is typically ensured by fulfilling Antenna Rules from the Design Manual, which make sure that at no time during the fabrication process a long metal wire connects to a transistor gate and not yet to the diffusion area of the driving logic gate.

- These Antenna Rules maybe complemented by Antenna Protections diodes inserted close to the victim gate when the above rule cannot be fulfilled just by playing upon metal routing.

- One difference between bulk CMOS and SOI has to do with the antenna effect mechanism: presence of BOx needs to be taken into account

**SOC Sign-Off Aspects**

Signing off a SOC design that has been ported from Bulk to FD-SOI will involve re-running a number of checks like Timing Checks, Design Rules Checks (incl. Antenna Rules), etc. on the design database. The design database needs to be updated to point to IPs and to library views updated for the FD-SOI technology (for example, re-characterized standard cells). Violations, if any, will have to be fixed by ECO (Engineering Change Order), as is classically done at the final steps of sign-off of a bulk design.

Source: SOI Consortium, “Considerations for Bulk CMOS to FDSOI Porting,” 2011
Bulk vs. FDSOI Transistors for Antenna Rules

- Gate is connected to the substrate
- Active area acts as a diode
- S/D pins are considered grounded: 2 pins transistor model (Gate and Substrate)

- Active (therefore Gate) is isolated from the substrate
- 3 pins transistor model (Gate – Source – Drain)
- Specific NAR coupled antenna methodology implemented
Body Bias Concept in FDSOI

- No area penalty compared to Bulk
- Reuse of Bulk design techniques
- Speed/Power control

Programmable Electrical Rule Checks (PERC) for FDSOI

- FDSOI increase complexity of bulk management because of the Body Bias options
- Specific rules in FDSOI are implemented due to the Multi-VT (HVT, RVT, LVT) and Back-Biasing
- Requires some specific voltage propagation rules to obtain the correct values per options