leti

innovation for industry

FDSOI developments

Olivier Faynot

OUTLINE

- Introduction
- International collaborations
- Technology description
- Device performance
- From Model to Design
- Summary

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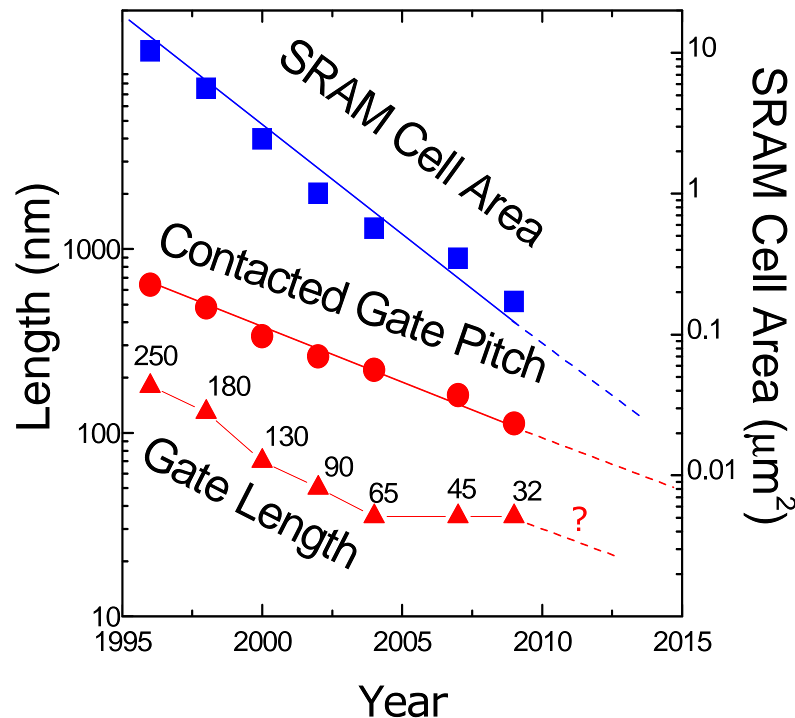
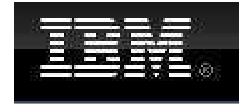
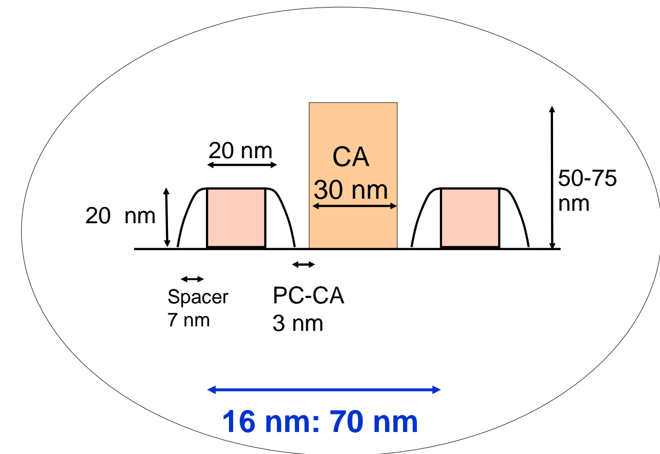
Introduction

- Tradeoff between Power/Performance/Variability slowed down the gate length reduction in Bulk



Ali Khakifirooz et al, FDSOI workshop, Taiwan 2011





Gate length reduction mandatory for 20nm and below

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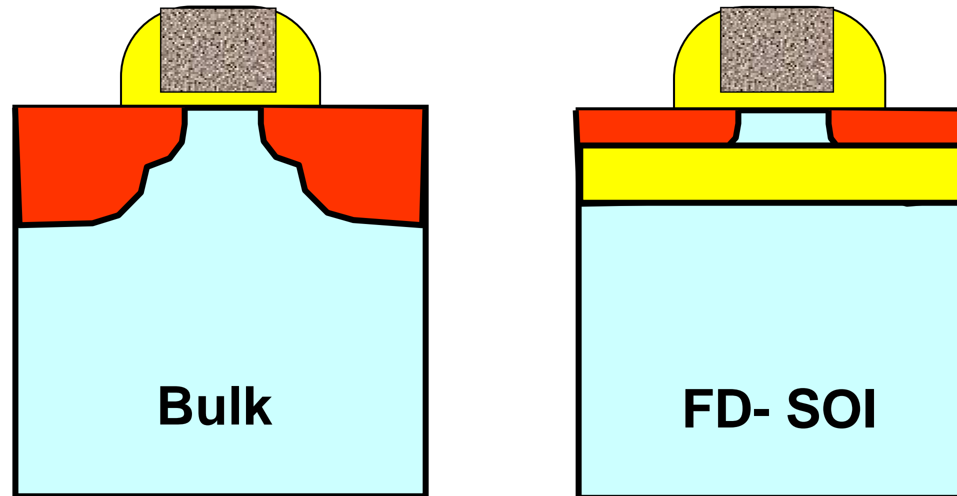
Introduction



- Use of SOI:
  - Improve the scalability further than Bulk
  - Reduce the variability thanks to undoped channel
  - Limit the static power and dynamic power
    - ➢ Low V_{DD} operation mandatory

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Process challenges and solutions

Challenge	Solutions
Access resistance	No Silicon loss during process No amorphization RSD epitaxy
Top Si Uniformity	Tight SOI manufacturer targets
Multiple VT	Gate workfunction, UTBOX
Strain for µ boost	SiGe, liners, Substrate

Also SPICE model and Circuit Design Infrastructure

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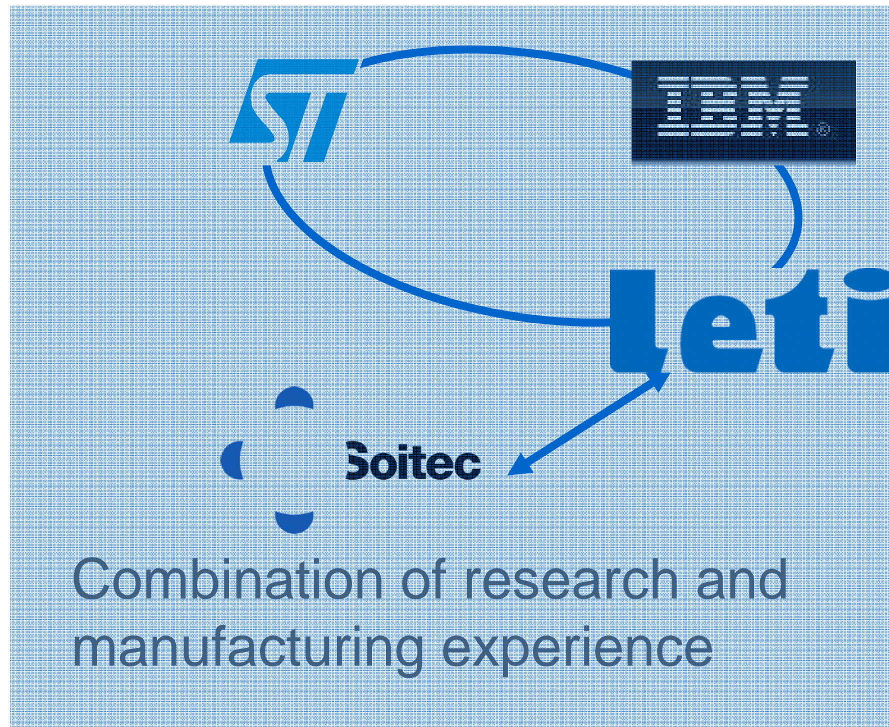
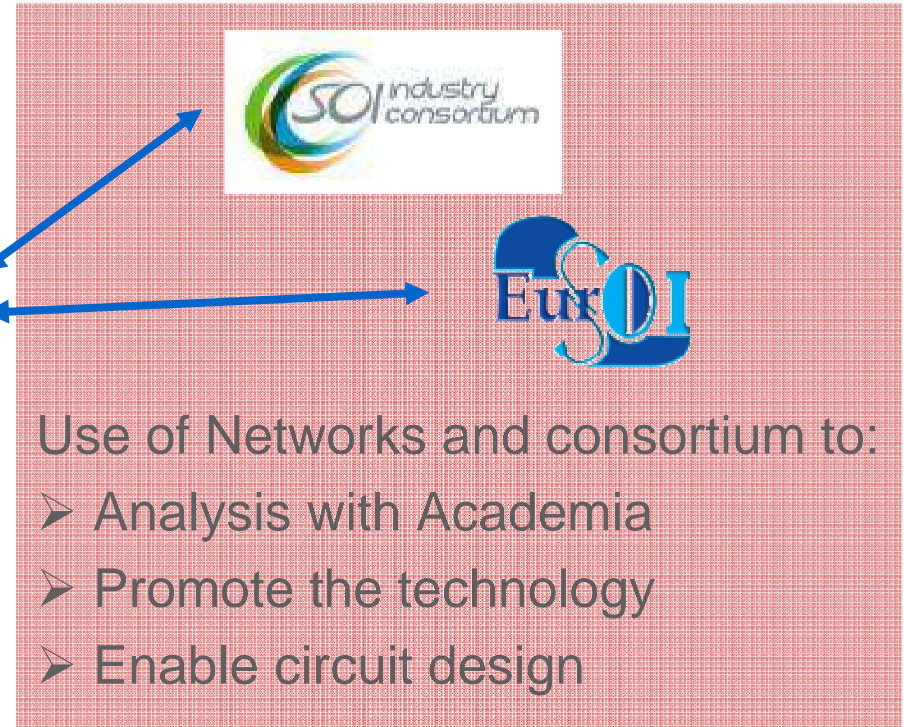
International Collaborations



Combination of research and manufacturing experience



Use of Networks and consortium to:

- Analysis with Academia
- Promote the technology
- Enable circuit design

Additional collaborations and support thanks to MEDEA+/CATRENE and ENIAC european projects (SILONIS, FOREMOST, DECISIF,MODERN…

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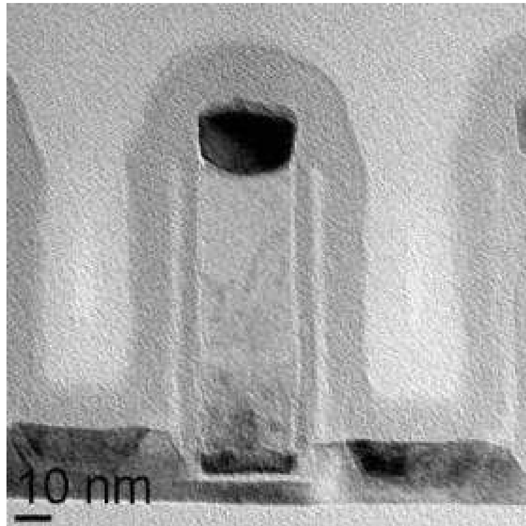
FDSOI Technology



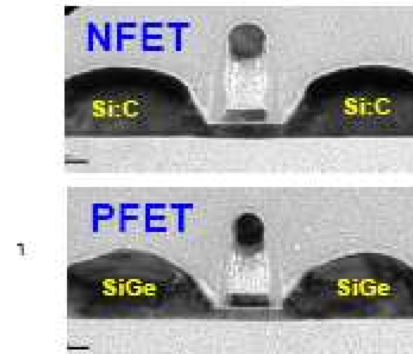
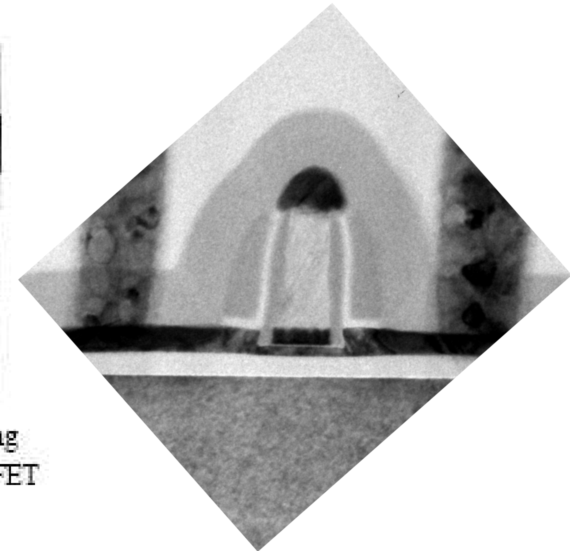


Fig. 2 TEM cross sections showing NFET with ISPD Si:C RSD and PFET with ISBD SiGe RSD.

K. Cheng et al, IEDM 2009



- **No channel doping, No Pocket implant**
- **Raised Source/Drain process**
- **Ultra-thin BOX Substrate option**

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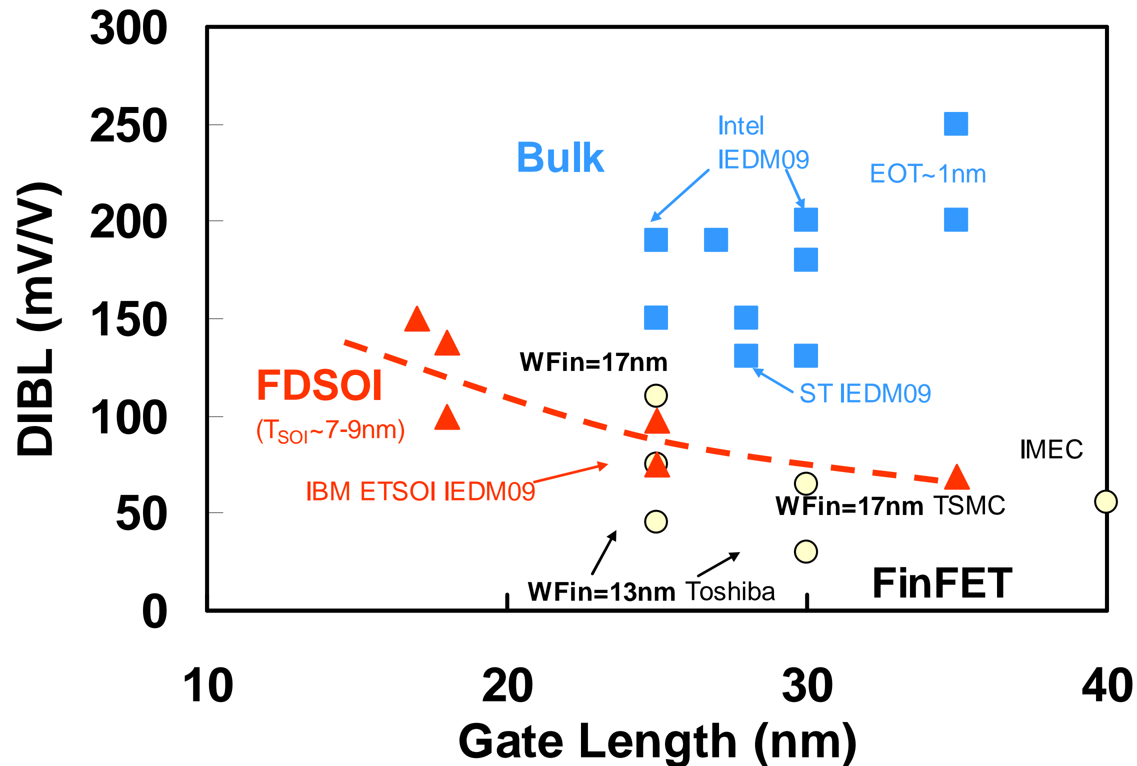
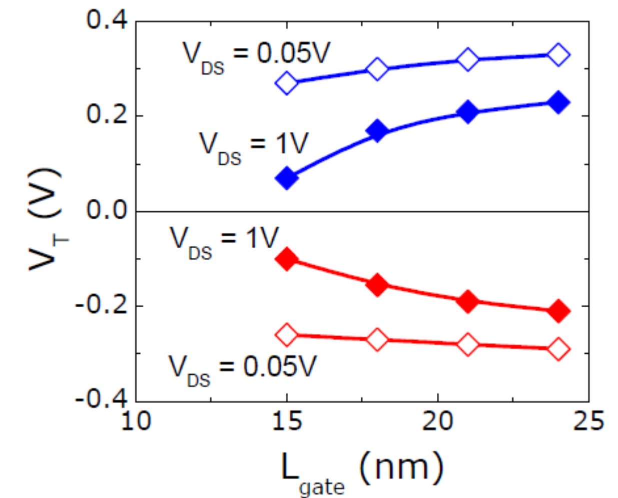
Electrostatic Performance





K. Cheng et al, VLSI 2011

- Enhanced electrostatic control compared to Bulk!
- Long channel DIBL~100 to 150mV/V for bulk vs. <50mV/V for FDSOI
- 15nm data already demonstrated

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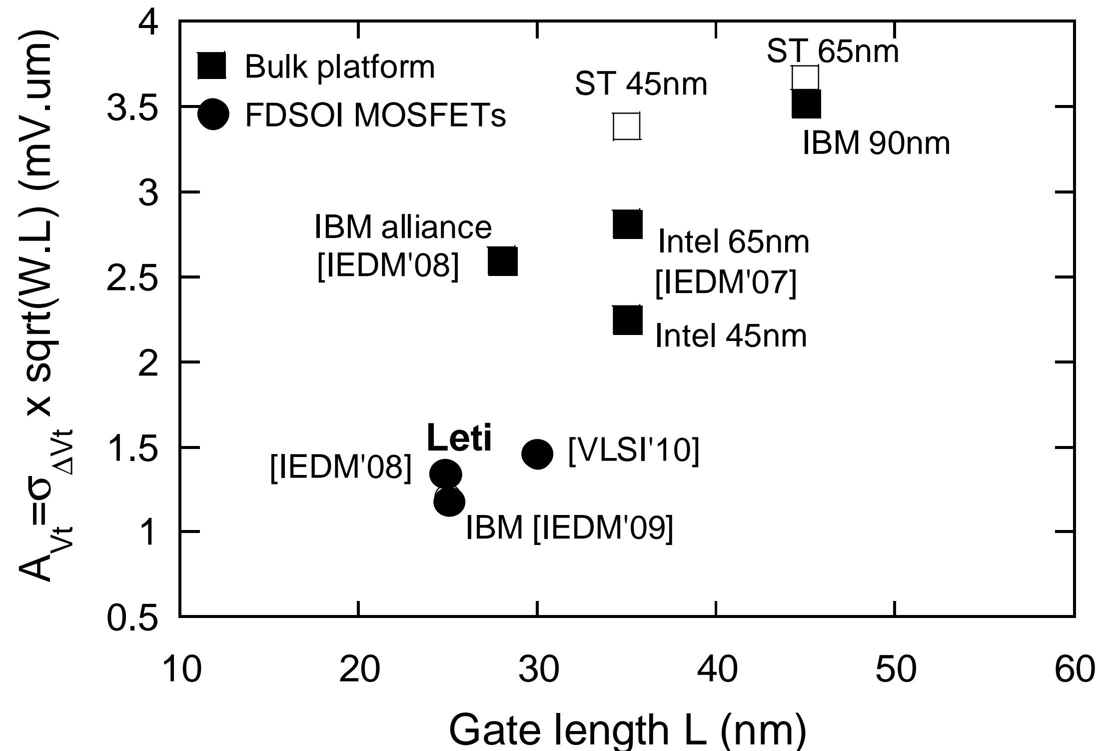
Variability- Benchmarking for several Technologies



- Record variability thanks to undoped channel
- Confirmed also by IBM

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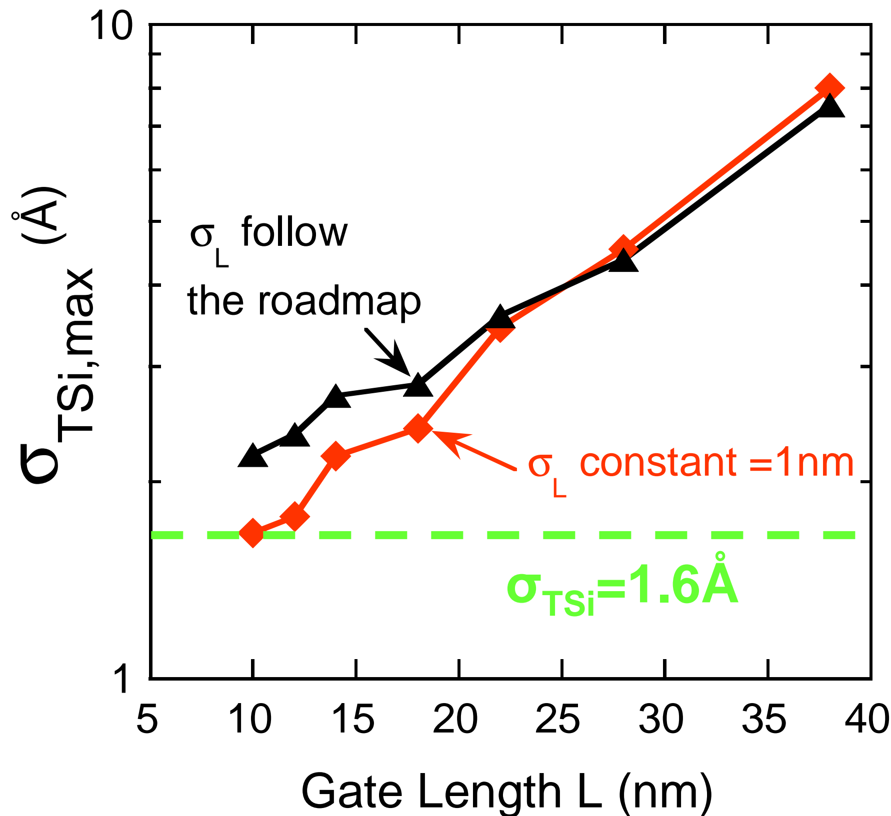
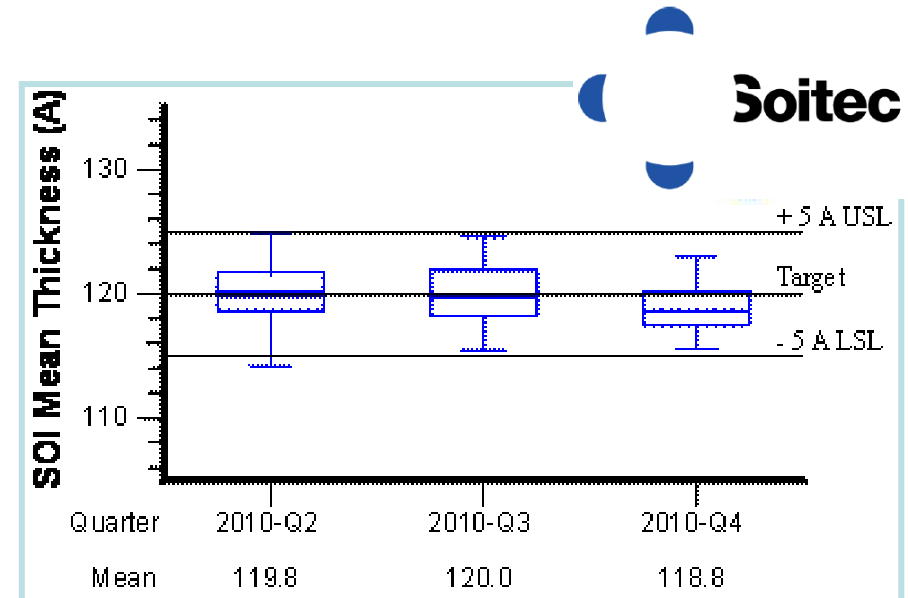
SOI thickness Unif. specs



French **NANOSMART** *project*



- σ~1.6Å required to get σV_T~3%V_{DD}
- Available wafers already on specifications!

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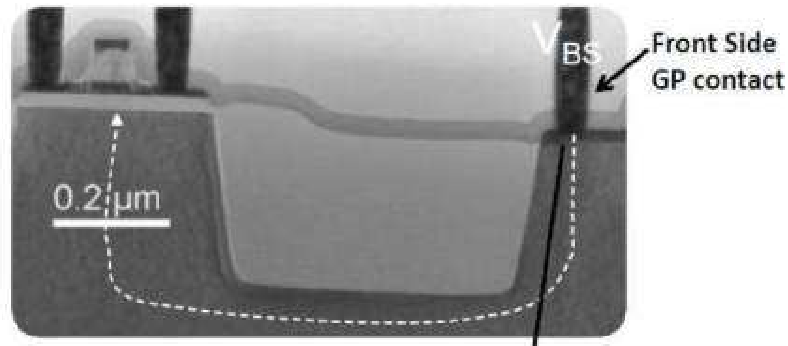
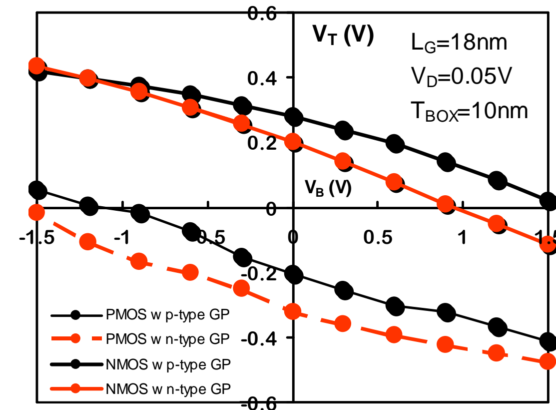
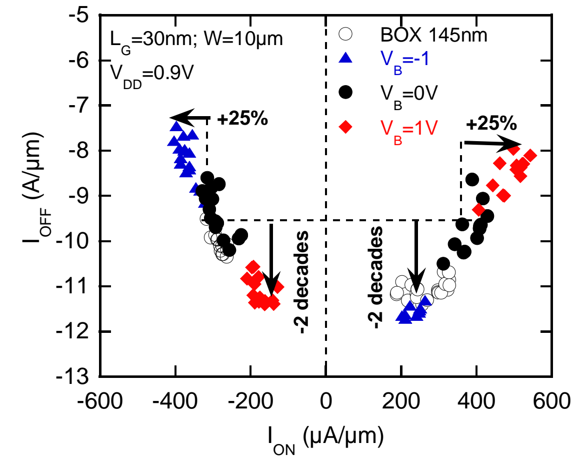
Back-gate contact







- No area penalty compared to Bulk
- Body factor maintained down to 18nm gate length
- Reuse of Bulk design techniques
- $I_{ON}(I_{OFF})$ modulation through Forward and Reverse Back bias

↳ Speed/Power control

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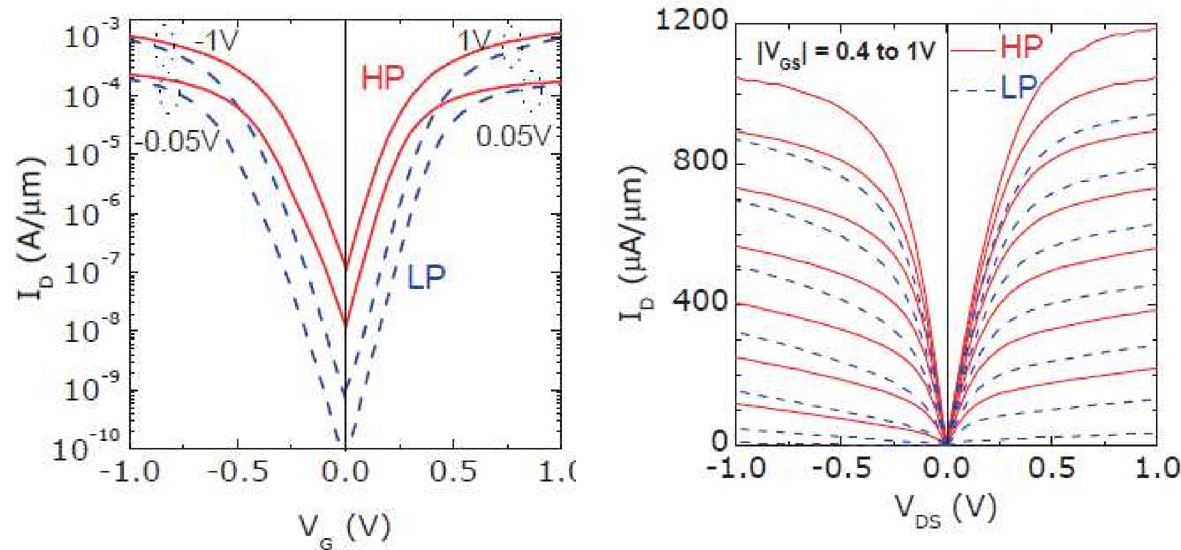
Drivability



V_{DD} = 1 V except Ref. [8] in which V_{DD} = 1.1 V

	ET SOI	Ref. [5]	Ref . [6]	Ref. [7]	Ref. [8]
L_G (nm)	22	30	28	34	?
Pitch (nm)	80-100	114	115	112.5	117
I_{OFF} (nA/µm)	1	0.45	2	1	1
NFET I_{ON} (µA/µm)	920	720	850	1120	680 @1.1 V
PFET I_{ON} (µA/µm)	880	410	450	870	470 @1.1 V

K. Cheng et al, VLSI 2011

- Competitive drivability
- Performance already demonstrated for LP and HP applications

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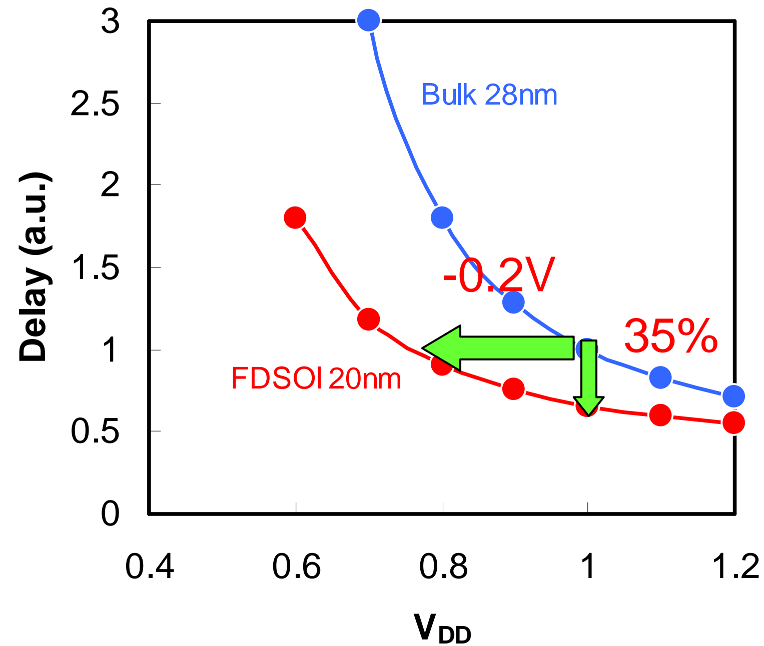
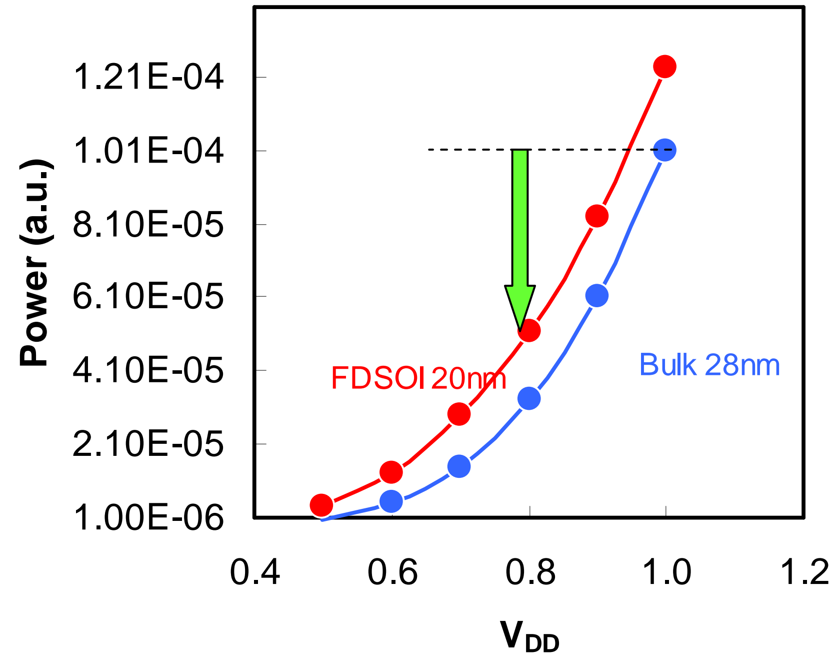
Speed/Power consumption gain

Low Power Technologies





- +35% speed gain at 20nm versus Bulk 28nm (same VDD)
- 0.2V V_{DD} reduction with SOI at same speed
- >50% Power reduction at constant speed

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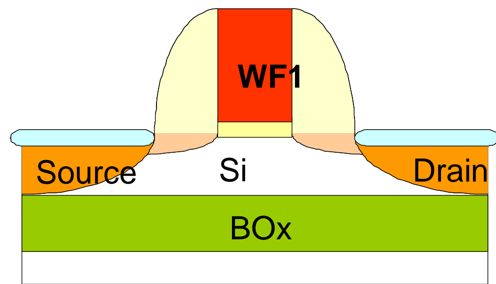
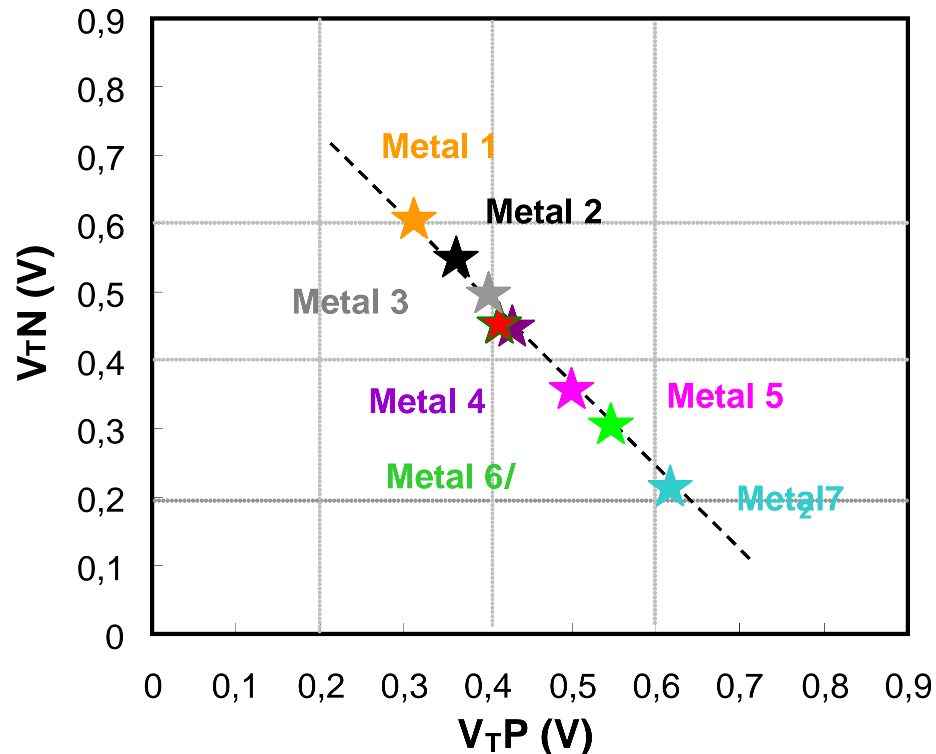
Multi-V_T aspects





Collaborations:

O. Weber et al, IEDM'10

- Band edge metals not suitable
- Quarter gap metal required for LVT, RVT, HVT N and PMOS

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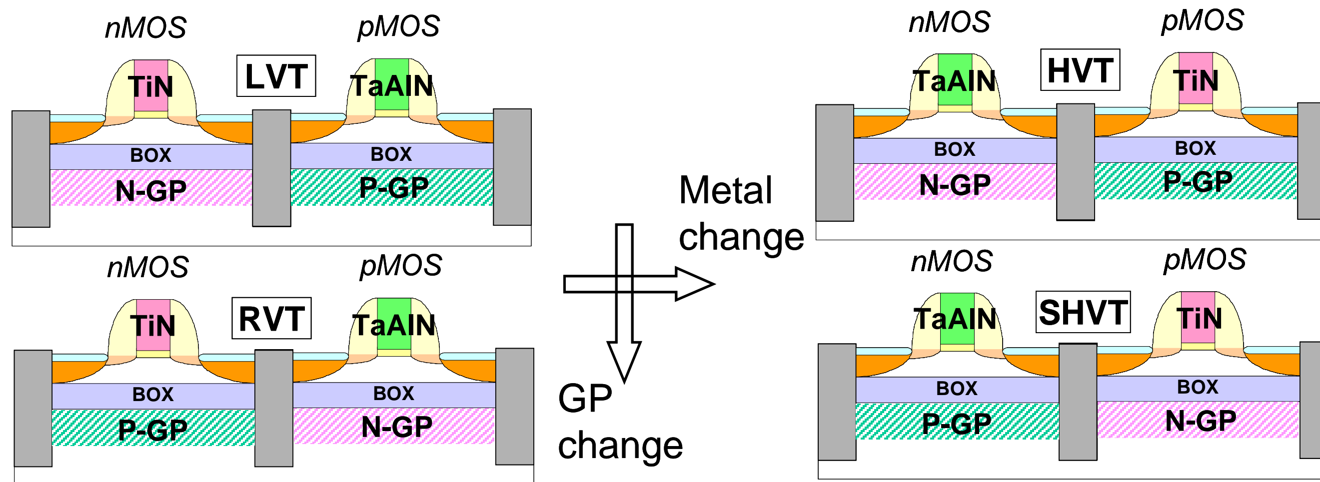
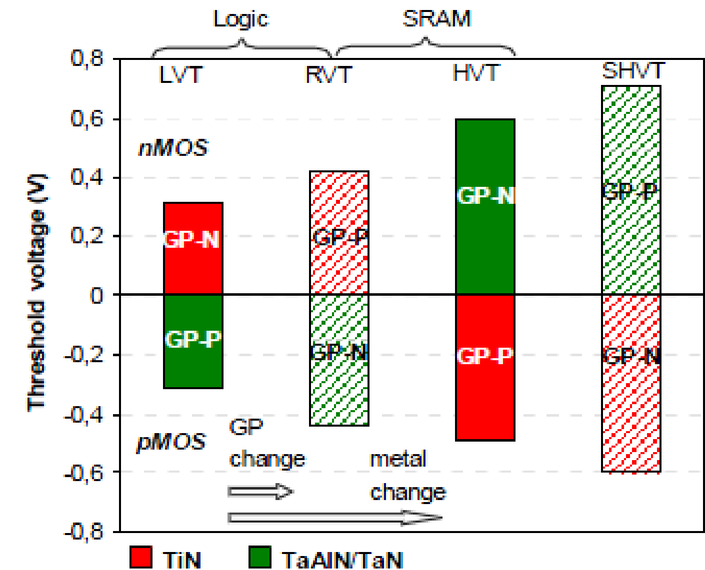
Multi-V_T aspects



- 2 gates and 2 GPs give $4V_{Ts}$ for both n&pFETs.
- All the required V_{Ts} for SoC are possible on UTBB



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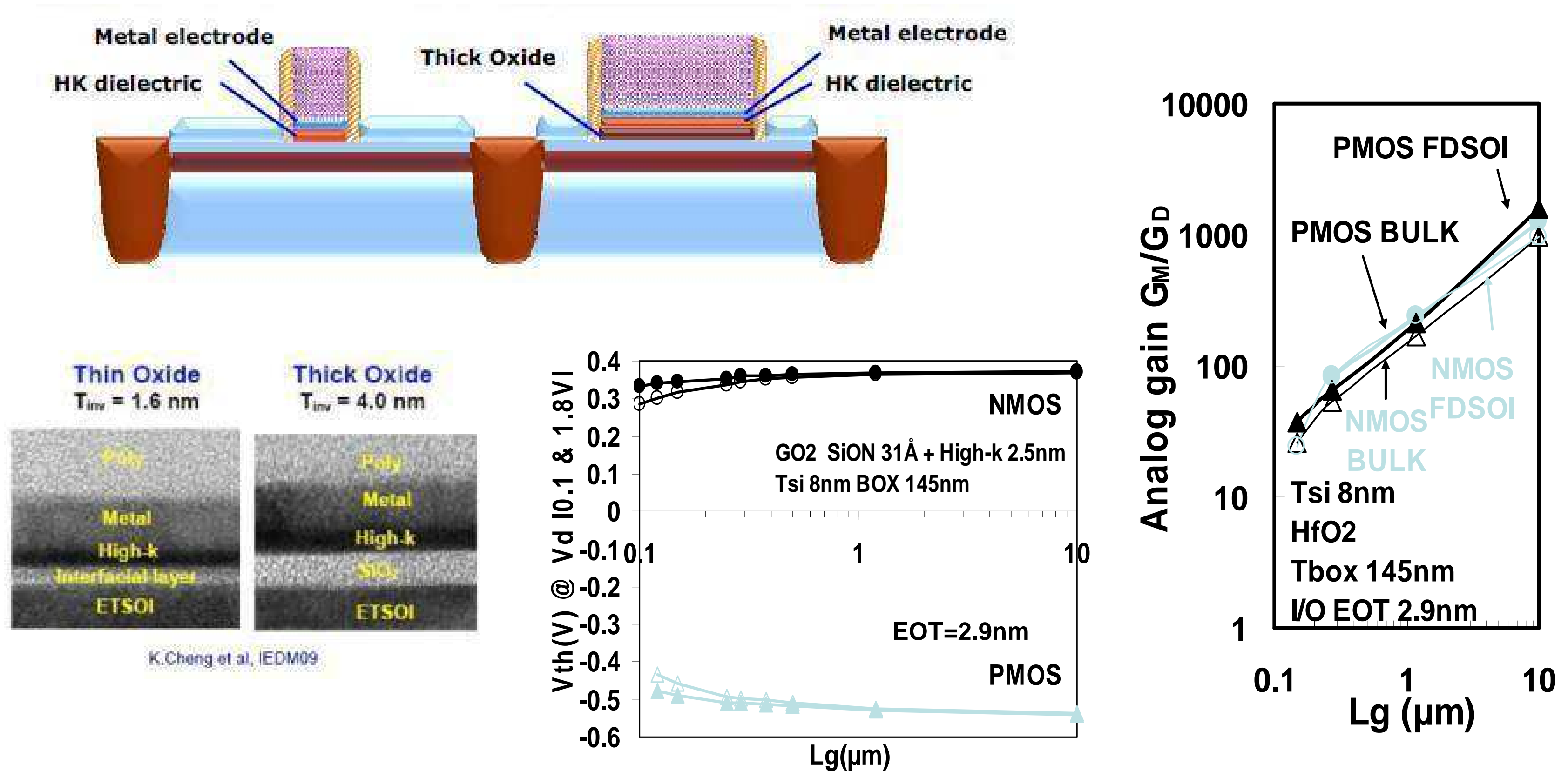
Analog I/O's



- Easy co-integration with Thin GOX devices
- Good performance and analog gain without any optimization (undoped channel)

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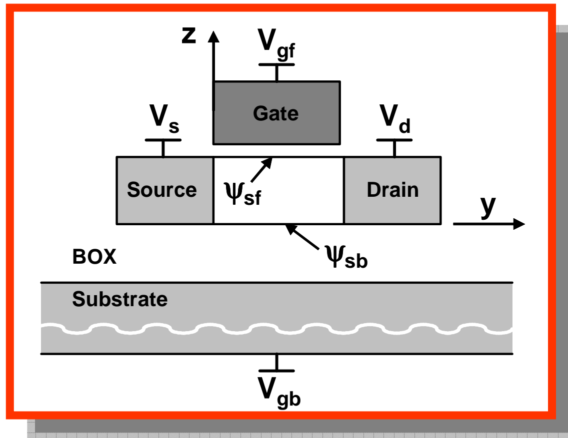
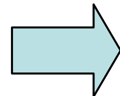
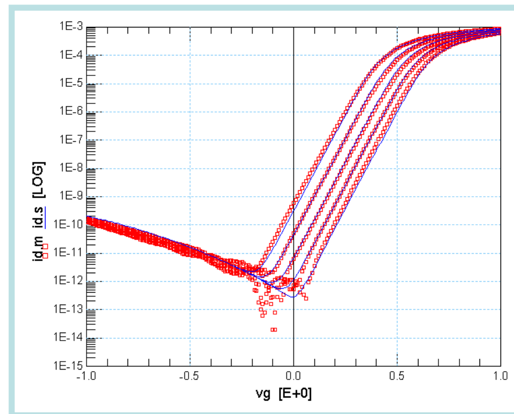
FDSOI SPICE model

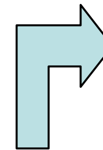
- Surface potential model

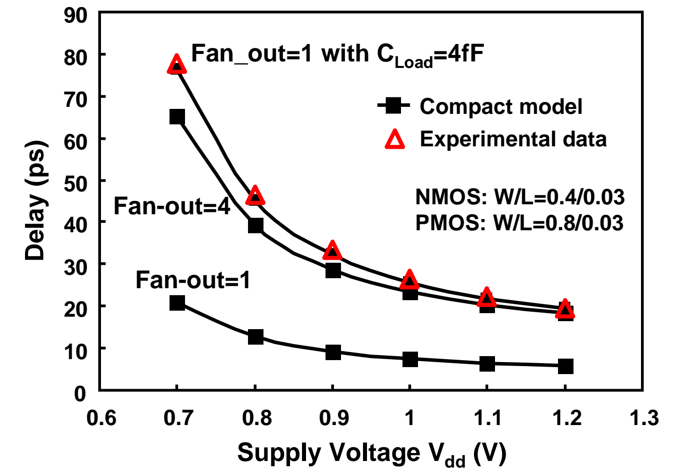


SOI related effects:
- -Interface coupling
- -Steeper Subthreshold slope
- -Self-Heating effect









Collaborations:

- Our target: To have a good FDSOI model standardized by CMC

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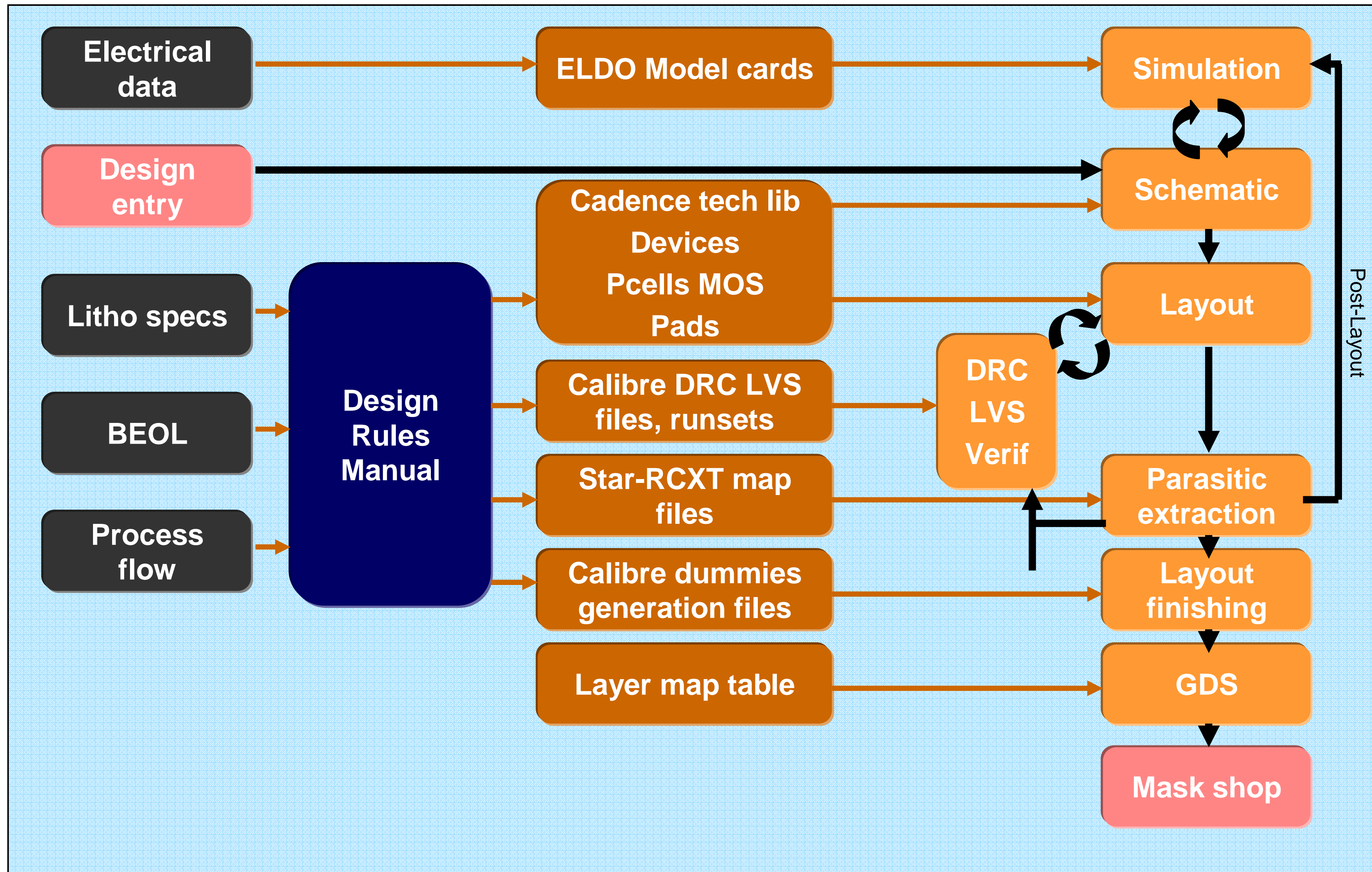
Circuit Design platform: Full custom Design flow



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Circuit Design platform: Full custom Design flow

MPW offer accessible via:

Already provided to:

University
of Southampton

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- **Trends and Summary**

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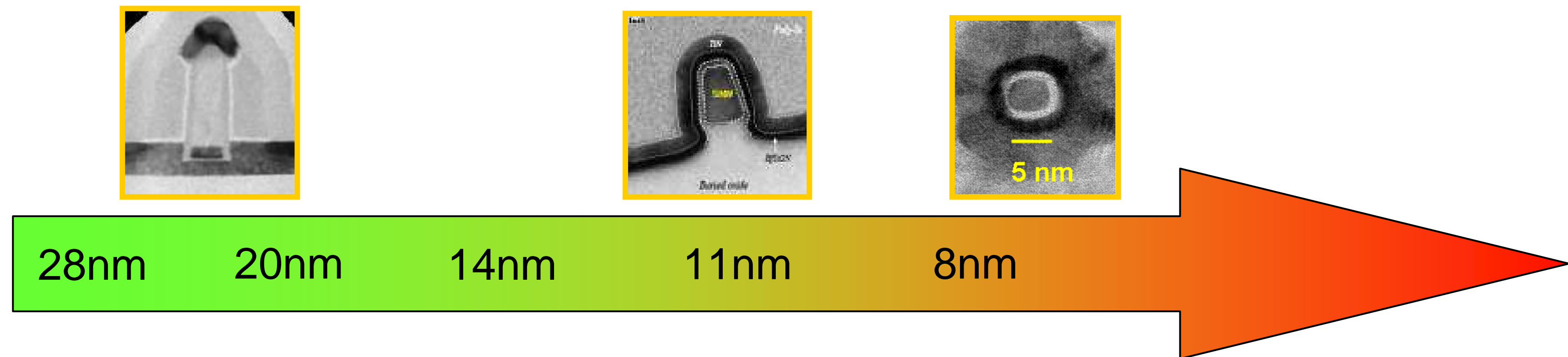
Trends for future nodes

Electrostatic considerations



- FDSOI scalability ensured down to L_G~14nm with UTBOX
- Both FinFET and FDSOI will merge towards Nanowire type of devices
- Around 8nm, Nanowires will provide perfect electrostatic control
- Alternative materials required to boost drivability

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Summary

- FDSOI Technology has strong advantages for sub20nm nodes
  - Improved electrostatic
  - Competitive drivability
  - Reduced variability
  - Additional elements demonstrated for SoC
- Circuit Design infrastructure built
- Strong international collaborations mandatory to accelerate developments

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Perspectives

- Incorporation of strain in FDSOI to address High Performance applications
- Use SiGe to boost hole mobility for PMOS
- Explore III-V materials for NMOS
- Develop 14 and 11nm infrastructures to enable design innovation

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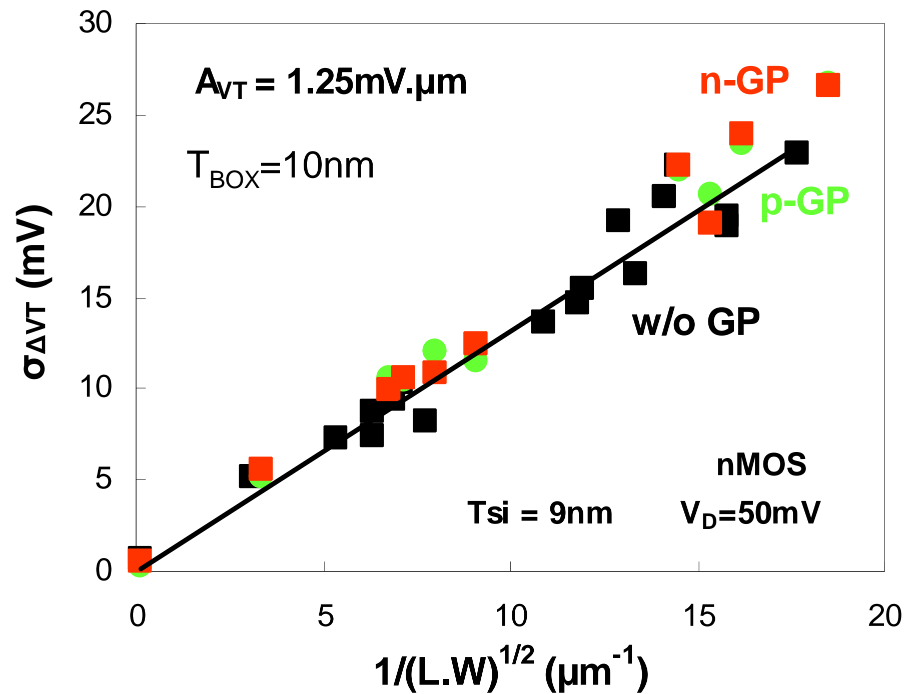
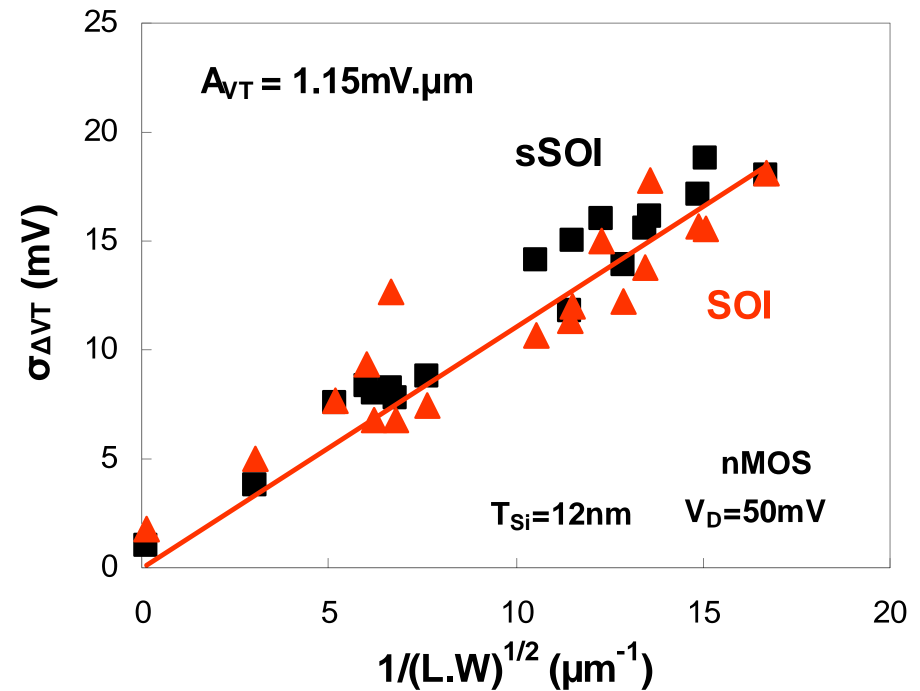
Merci de votre attention

Variability- Impact of SOI wafer





- Same variability on Thick BOX and Thin BOX wafers
- No impact of Ground Plane implantation (n & p-type)
- Same variability on strained-SOI and standard-SOI wafers

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