FDSOI design at Leti
A TTM accelerator for your ULP ICs

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Agenda

FDSOI Ultra Low Power ICs

Our design experience & skills

Our FDSOI design offer
ULP ICs – performance vs power

- Traditionally, designing an ultra low power IC meant

  Low Consumption ⇔ Low Performance

- With FDSOI technology and specific design optimizations we maximize the performance vs. power consumption equation

- With FDSOI

  Same Performance ⇔ Lower Power Consumption
  Same Power Consumption ⇔ Higher Performance
FDSOI : new opportunities

- FDSOI enables new opportunities
  - Both in digital & RF/mixed signal design
  - ULP design scenarios to combine processing power, communications and energy efficiency

- Using FDSOI and an optimized design CEA-Leti can help you create world class leading energy efficient ICs

- A few examples
  - Ultra Low Power IoT node
  - Ultra Low Power, high functionality portable products (medical, consumer, ...)
  - Green computing (microservers, HPC, ...)
FDSOI intrinsic advantages for ULP design

UTBB FD-SOI Max Frequency vs. BULK

Vdd (V)

Frequency (MHz)

LDPC 6T-SRAM functional down to 0.41V

UTBB FD-SOI

noBB

FBB=0.3V

BULK-LP (ref)

83%

43%

29%

UTBB FD-SOI Total Power vs. BULK

Vdd: 0.6V to 1.5V step 100mV

Normalized Total Power (a.u.)

0.6V

1V

1.3V

FBB=0.3V

noBB

+19%

-33%

-35%

+18%
FDSOI design & optimizations go further

- FDSOI has intrinsic ULP benefits

- BUT optimizing the design for FDSOI leads to even greater power/performance gains

**UTBB-FDSOI performance gain versus conventional Bulk CMOS technology. Blue: no body biasing, Green: FBB = +1V.**

- FBB up to +2V and $F_{\text{MAX}}$ tracking:
  - $\uparrow$ frequency up to 460MHz at minimum voltage

**UTBB-FDSOI performance gain versus conventional Bulk CMOS technology. Blue: no body biasing, Green: FBB = +1V.**

- FBB up to +2V and $F_{\text{MAX}}$ tracking:
  - $\uparrow$ frequency up to 59% (target 100pJ/cycle)
  - $\searrow$ Energy by 20% (target 1.7 GHz)
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FDSOI Ultra Low Power ICs

Our design experience & skills

Our FDSOI design offer
CEA-Leti design team skills & experience

- FDSOI Technology & Design platforms
  - More than 20 years experience on SOI development
  - Experts in FDSOI design & technology

FDSOI Design & Embedded Systems
- 180 designers
- 3,000 m² working space
- 42 chips in 2013
- 20 M€ CAD tools

Micro & nanoelectronics
- 400 engineers & technicians
- 7,200 m² clean rooms
- 200 & 300 mm equipment
- 500 M€ investment

Nanocharacterization
- 80 researchers
- 3,200 m²
- ~40 heavy equipment
- 30 M€ investment
Our main competitive advantages

- Unique FDSOI local ecosystem
  - Technology knowledge
  - Design & design flow expertise
  - Extensive emulation & simulation expertise & capabilities
  - Prototype testing & manufacturing
  - Industrial production with local partners (MPW runs available in 2015)

- Wide range design skills
  - Advanced Digital
  - RF design skills
  - Sensor interfaces
Our main competitive advantages – cont’d

- Deep knowledge of FDSOI technology & expert design skills
  - Unique Hardware & Software co-design skills at your service

- FDSOI power management IPs & optimization methodologies
  - Vbb, Vdd, F
  - Polybiasing best strategy

- Specialized memory design
  - Ultra low voltage
  - Ultra wide voltage range
  - Advanced research on RRAM technology mix
One example: FRISBEE, FDSOI 28nm 32bits DSP

High Performance – Very Low Power

- 1mm², 2M gates, UTBB 28nm FDSOI
- Fmax 2.6GHz @ 1.3V
- 370mW @ 1V, 62pJ/op @ 0.53V

Dynamic voltage range

- 0.39v to 1.3v

Working Freq. = 460MHz @ 397mV

- +900% @ 0.5V (wrt SotA)
- +90% @ 1V (wrt SotA)

Top : comparison with state of the art,
Medium : Chip layout
Bottom : FRISBEE DSP demonstrator
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FDSOI Ultra Low Power ICs

Our design experience & skills

Our FDSOI design offer
How do we help you?

Option 1

Client Specs

Option 2

Client Design

FDSOI Design

Leti Support

Option 3

Client FDSOI Design

FDSOI Optimization

Leti Ips & Know-How

Verification

Leti Emulator & Simulator

Prototype

Characterization & Test

Mass Production

MPW Runs

Leti or Client

Partner from ecosystem

Leti Support
Offers side by side

- 3 offers to help you with designing your ULP IC

**TTM acceleration**
- Accelerating your FDSOI design TTM
- Basic FDSOI transfer

**TTM acceleration & optimization**
- Accelerating your FDSOI design TTM
- Basic FDSOI optimization

**TTM acceleration & FDSOI expertise**
- Accelerating your FDSOI design TTM
- Advanced FDSOI optimizations
- Symbiotic FDSOI know-how transfer
TTM acceleration

- CEA-Leti transfers your design to FDSOI without FDSOI design optimizations
- Technical report & final FDSOI design delivered

**Pros**

- Inexpensive
- TTM greatly reduced
- HW intrinsic perf vs. power benefits

**Cons**

- Little FDSOI design know-how transfer
- No FDSOI design optimization benefits
TTM acceleration & optimization

- CEA-Leti transfers your design to FDSOI and applies basic FDSOI optimizations (back biasing)
- Technical report & final FDSOI design delivered

Economically priced
- TTM reduced
- Basic FDSOI design
- Know-how transfer
- HW + basic FDSOI design perf vs. power benefits

Full FDSOI benefits not reached
TTM acceleration & FDSOI expertise

- CEA-Leti and client design team work together on porting the design to FDSOI & applying full range of FDSOI optimizations
- Common lab, full know-how transfer

TTM minimized (design teams work together)
Maximal know-how transfer
Advanced IP
HW + advanced FDSOI design perf vs. power benefits

Higher price
Summary of FDSOI offer

- 3 offers to help you with designing your ULP IC

- An entry point based on your need
Thank you for your attention!