

CEA-Leti Reports Progress in Computing, Medical Electronics, Communications, and Other Fields at ISSCC 2011

CEA-Leti Device-Design Experts Available to Discuss Emerging Developments in 60GHz CMOS Design, Design for Imaging and Multicore Digital Chips

GRENOBLE, France – Feb. 08, 2011 – CEA-Leti researchers and their partners will report on projects that address fundamental challenges facing next-generation computing, medical diagnosis, communications, and portable electronics at ISSCC 2011, Feb. 20-24, in San Francisco, Calif.

The ISSCC (International Solid-State Circuits Conference) is the premier forum for presenting advances in solid-state circuits and systems-on-a-chip. The conference theme this year is “Electronics for Healthy Living,” highlighting integrated circuits for biomedical systems.

One paper featuring CEA-Leti authors includes work on RF (60GHz) communication chips performed in connection with chipmaker STMicroelectronics to target 60GHz Wireless HD Applications. CEA-Leti demonstrates that it is possible to integrate in standard low-cost CMOS 65nm technology a low-power system-on-chip working in the 60GHz frequency band with a data rate up to 3.8Gbps. The data rate is 70 times higher than traditional 54Mbps WiFi technology. This technology will open new opportunities for fast up-and-down loading applications.

Two of CEA-Leti’s top presentations deal with imaging devices for professional applications: a Thz imager built with a low-cost technology, and an infrared imaging array capable of returning an image with a thermal resolution of 1 to 2 mK at ambient temperature. In keeping with its strategic focus on bringing innovations from the development stage to manufacturability, CEA-Leti has expanded its optronics efforts from the boosting of sensor performance to creating new architectures and design technologies that enable easier integration into system-level products.

In addition to the presentations listed below, two CEA-Leti specialists — Dr. Ahmed Jerraya, head of the Strategic Design Programs; and Michel Durr, Analog and RF IC Design Program manager — will be available for meetings with journalists during the conference. Interviews can be arranged through CEA-Leti’s communications team, to discuss emerging developments in:

- **60GHz CMOS design.** CEA-Leti has designed many circuits in the 60GHz millimeter range in European projects and industrial partnerships with STMicroelectronics and NEC. This work has resulted in several reviews and papers in major international conference proceedings, such as ISSCC, Radio Frequency Integrated Circuits (RFIC) and the Journal of Solid State Circuits (JSSC).
- **Design for imaging.** Current research subjects deal with 3D integration to enable massively parallel image processing, large-area imaging sensors obtained by stitching processing for medical applications (X-rays), and with 3D vision with infrared imaging array derived from a time-of-flight computing.

CEA-Leti research projects include infrared, visible, X-rays and gamma displays and sensors for applications in defense, security, health, cameras, phones and

gaming. CEA-Leti's design emphasis is on ultra-low noise, low-power, enhanced analog-to-digital and digital-to-analog converters, advanced architecture for signal processing and integrated image processing.

- **Multicore digital chips.** CEA-Leti's Network-on-Chip (NOC) brings a notable improvement over conventional bus systems. As IC complexity increases, more processing elements are used in parallel to improve the computation performance (multi-core processors), and the bus approach with shared connections between all the computing cores limits device performance. In an NOC, connections are point-to-point links operating simultaneously. This high level of parallelism will greatly improve the scalability of SoCs (adding new computing cores will not lead to re-design of the whole chip), their flexibility (routing possibility between the different cores) and their power efficiency (due to short connections).

The GALS approach developed in CEA-Leti's NoC implementation is the main differentiating feature with other concurrent teams. An easy Lego-like chip assembly allows a decoupling between the different processing cores of the NoC, thus allowing fine-grain power management, while reducing the time-to-market. All these developments will be used in next-generation telecom embedded systems such as 3GPP-LTE (Third Generation Partnership Project – Long Term Evolution) and software-defined radio; or in multimedia chips, in image enhancement, for instance.

Topics covered by CEA-Leti and its partners' papers include:

Monday, Feb. 21

3:45 p.m., Session 2 "Technologies for Health"

- A Broadband THZ Imager in a Low-Cost CMOS Technology

A CMOS Imager for Terahertz imaging is presented. A MOSFET is coupled to a bow-tie antenna. Self-mixing allows direct conversion to the low frequency band used for light modulation. The imager includes an in-pixel low noise amplifier, and multiplexing circuitry for single-video output. Measurement results are presented with electrical performances and images.

3:45 p.m., Session 6 "Sensors & Energy Harvesting"

- A $\pm 1.5\%$ Nonlinearity 0.1-to-100a Shunt Current Sensor Based on a 6kv Isolated Micro-Transformer for Electrical Vehicles and Home Automation

An integrated current sensor including a shunt, 2 micro-transformers for 6kV isolation, a chopper IC and a readout IC is presented. Current measurements are performed with a $\pm 1.5\%$ nonlinearity over a 0.1-to-100 A range. The signal BW ranges from DC to 20kHz, and the overall power consumption is 16mW. The microsystem fits in a 13x7.6mm² SO20 package.

Tuesday, Feb. 22

9 a.m., Session 9 "Wireless & MM-Wave Connectivity"

- A 65nm CMOS Fully Integrated Transceiver Module for 60GHz Wireless HD Applications

A fully integrated Wireless HD-compatible 60GHz transceiver module covering the four standard channels is presented. The 65nm CMOS die, external PA and high aperture antennas are flip-chipped a top a low cost HTCC substrate using an industrial packaging line. The module achieves a 16-QAM OFDM modulation wireless link over 1 meter distance.

5 p.m., Session 12 “Design in Emerging Technologies”

- GHz-Range Continuous-Time Programmable Digital FIR with Power Dissipation that Automatically Adapts to Signal Activity (with Columbia University)

A continuous-time 3b 6-tap ADC/DSP-DAC system is realized in 65nm CMOS for GHz applications with a 0.8-to-3.2GHz bandwidth, occupying a core area of 0.08mm². It has activity-dependent alias-free sampling and power dissipation from 1.1 to 10mW, achieving a maximum effective sampling rate of 45GS/s with an SNDR of 20dB.

5 p.m., Session 15 “High-Performance SoCs & Components”

- A Side-channel and Fault-Attack Resistant AES Circuit Working on Duplicated Complemented Values

A secure AES chip is implemented in HCMOS9gp 0.13μm STM technology. The counter-measures are based on duplication (for detecting faults) and work on complemented values in parallel (for protecting against side channel attacks). The chip is tested against side-channel and fault attacks and is resistant to both, illustrating the efficiency of the approach.

Wednesday, Feb. 23,

11 a.m., Session 19 “Low-Power Digital Techniques”

- Comparison of 65nm LP Bulk and LP PD-SOI with Adaptive Power Gate Body Bias for an LDPC Codec (with STMicroelectronics)

An 802.11n 693Mb/s LDPC codec is implemented in the first available 65nm 3Vt 7ML Low-Power Partially Depleted SOI (LP PD-SOI) technology. Low resistivity forward-body-biasing power-switching techniques are introduced in PD-SOI to reduce the leakage current by 52.4% vs. bulk. We also increase frequency by 20% at 1.2V and decrease dynamic power by 30% at 360MHz.

9:15 a.m., Session 23 “Image Sensors”

- A 320×256 90dB SnR and 25μm-Pixel-Pitch Infrared Image Sensor

A 320×256 pixel, 25μm pixel pitch, 0.18μm CMOS readout IC with a 15b pixel-level ADC for cooled hybrid infrared image sensors. The chip is hybridized with a long-wave infrared detector fabricated in HgCdTe via indium bump bonding and yields 90dB SNR at 50fps operation in a snapshot mode.

About CEA-Leti

CEA is a French research and technology organization, with activities in four main areas: energy, information technologies, healthcare technologies and defence and security. Within CEA, the Laboratory for Electronics & Information Technology (CEA-Leti) works with companies in order to increase their competitiveness through technological innovation and transfers. CEA-Leti is focused on micro and nanotechnologies and their applications, from wireless devices and systems, to biology and healthcare or photonics. Nanoelectronics and microsystems (MEMS) are at the core of its activities. As a major player in MINATEC campus, CEA-Leti operates 8,000-m² state-of-the-art clean rooms, on 24/7 mode, on 200mm and 300mm wafer standards. With 1,200 employees, CEA-Leti trains more than 150 Ph.D. students and hosts 200 assignees from partner companies. Strongly committed to the creation of value for the industry, CEA-Leti puts a strong emphasis on intellectual property and owns more than 1,500 patent families.

For more information, visit www.leti.fr.

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